CMOS Inverter

Vishal Saxena
ECE, Boise State University

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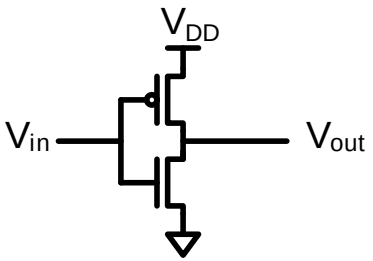
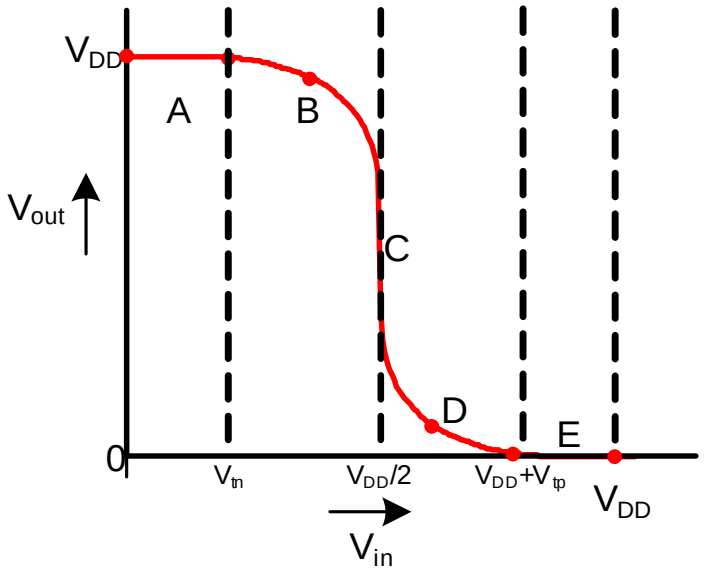
Inverter Operation Regions

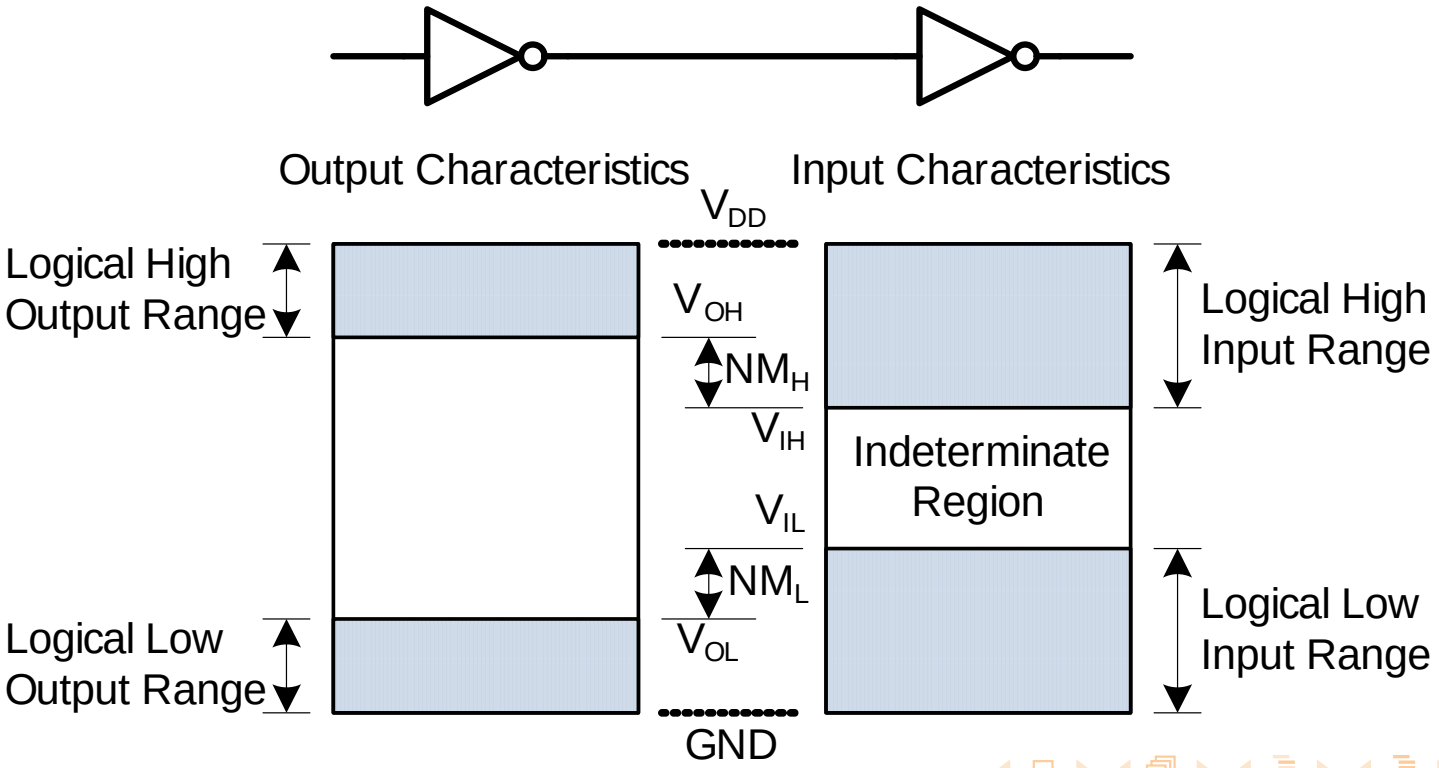
Region	NMOS	PMOS
A	Cutoff	Triode
B	Saturation	Triode
C	Saturation	Saturation
D	Triode	Saturation
E	Triode	Cutoff





Noise Margin

- How much noise can a gate input see before it does not recognise the output?
  - Noise margins of a digital gate indicate how well it will perform with noisy conditions



Noise Margin

- $NM_H = V_{IH} - V_{OH}$
  - HIGH noise margin
- $NM_L = V_{IL} - V_{OL}$
  - LOW noise margin
  - V_{IH} = minimum HIGH input voltage
  - V_{IL} = maximum LOW input voltage
  - V_{OH} = minimum HIGH output voltage
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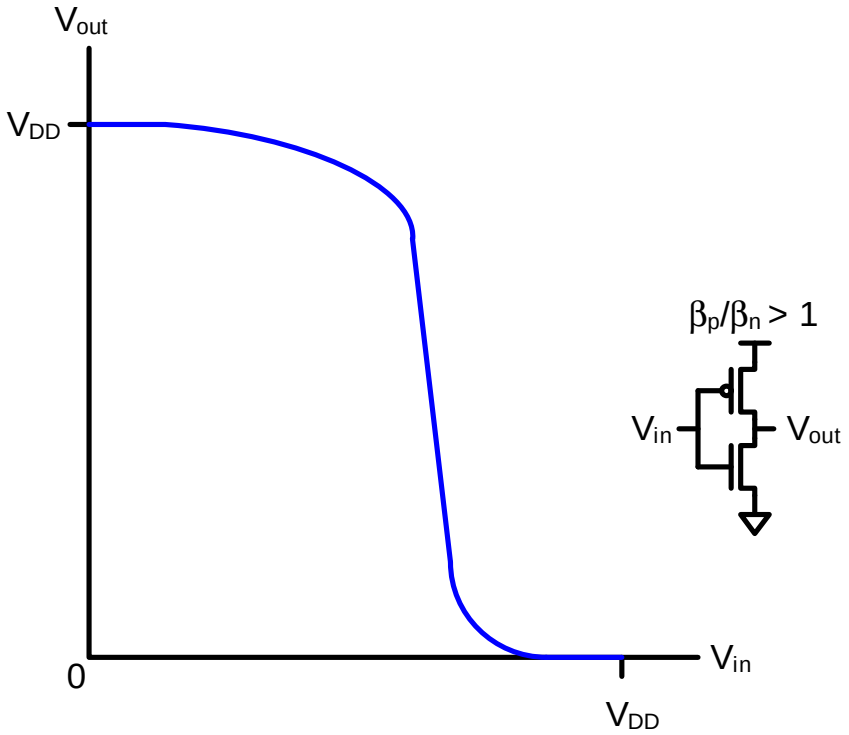
Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristics



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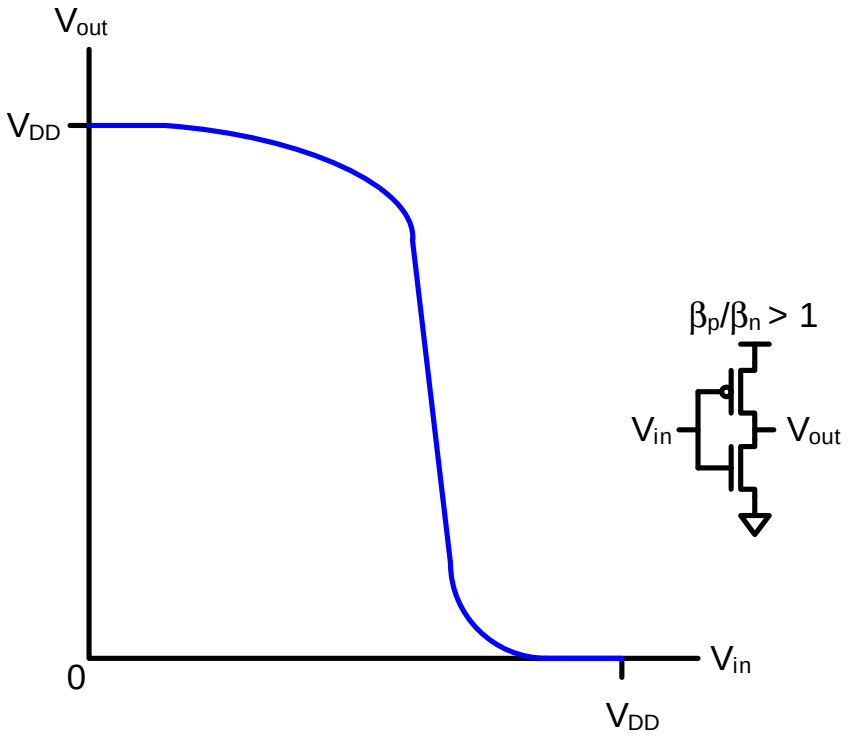

Logic Levels

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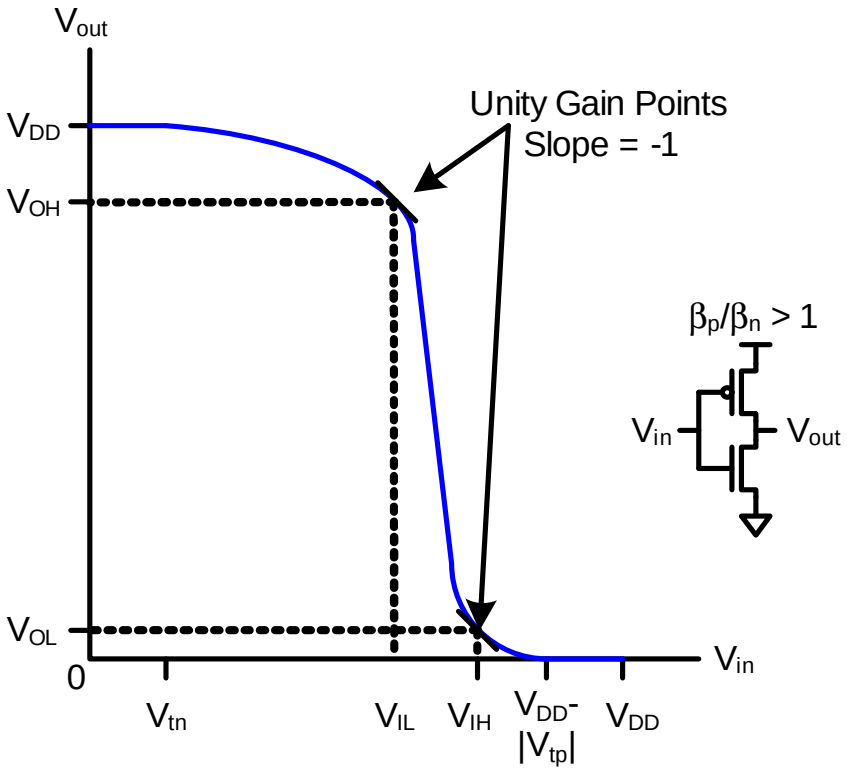
  - gate should be able to regenerate the levels



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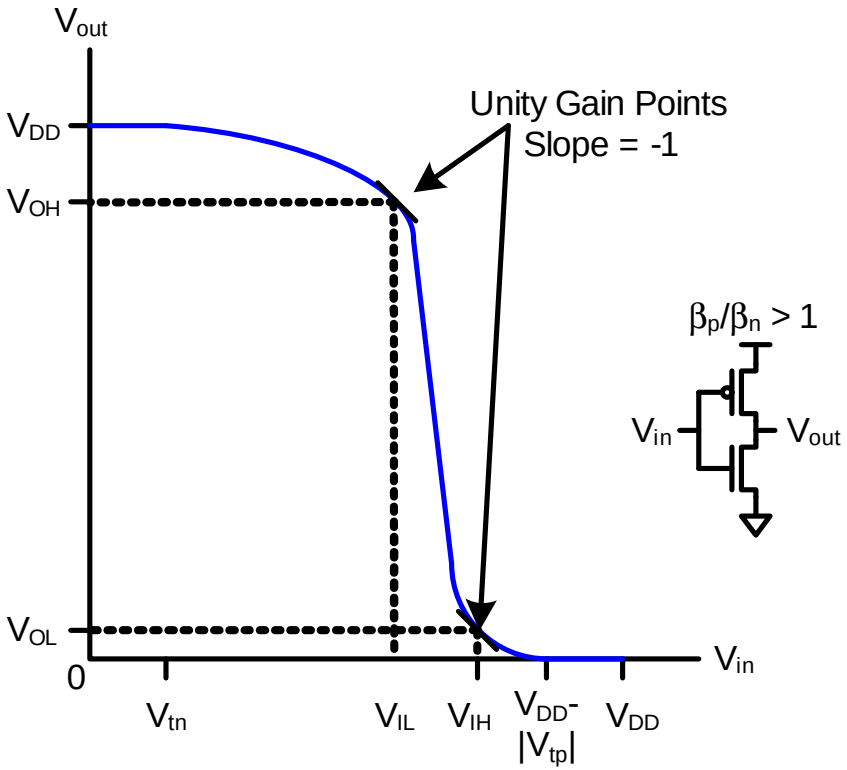

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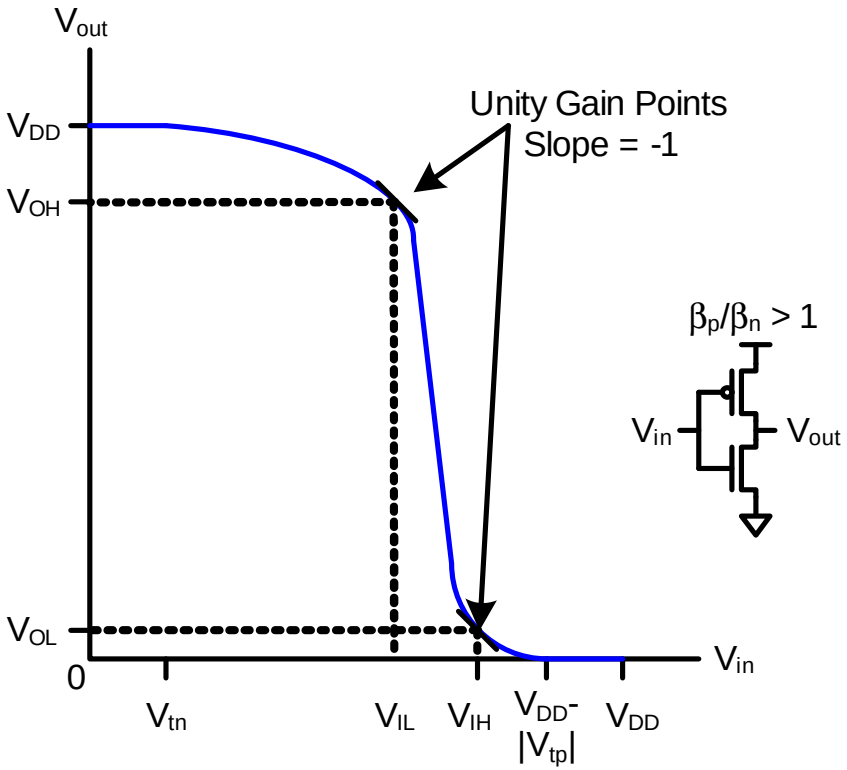

- If $\frac{\beta_n}{\beta_p} \neq 1$, inverter's switching point (V_{SP}) will move from the ideal value of $\frac{V_{DD}}{2}$
  - called skewed gate