ECE 445 INTRO TO VLSI DESIGN

PAD FRAME BASICS

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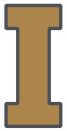

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BOND PAD

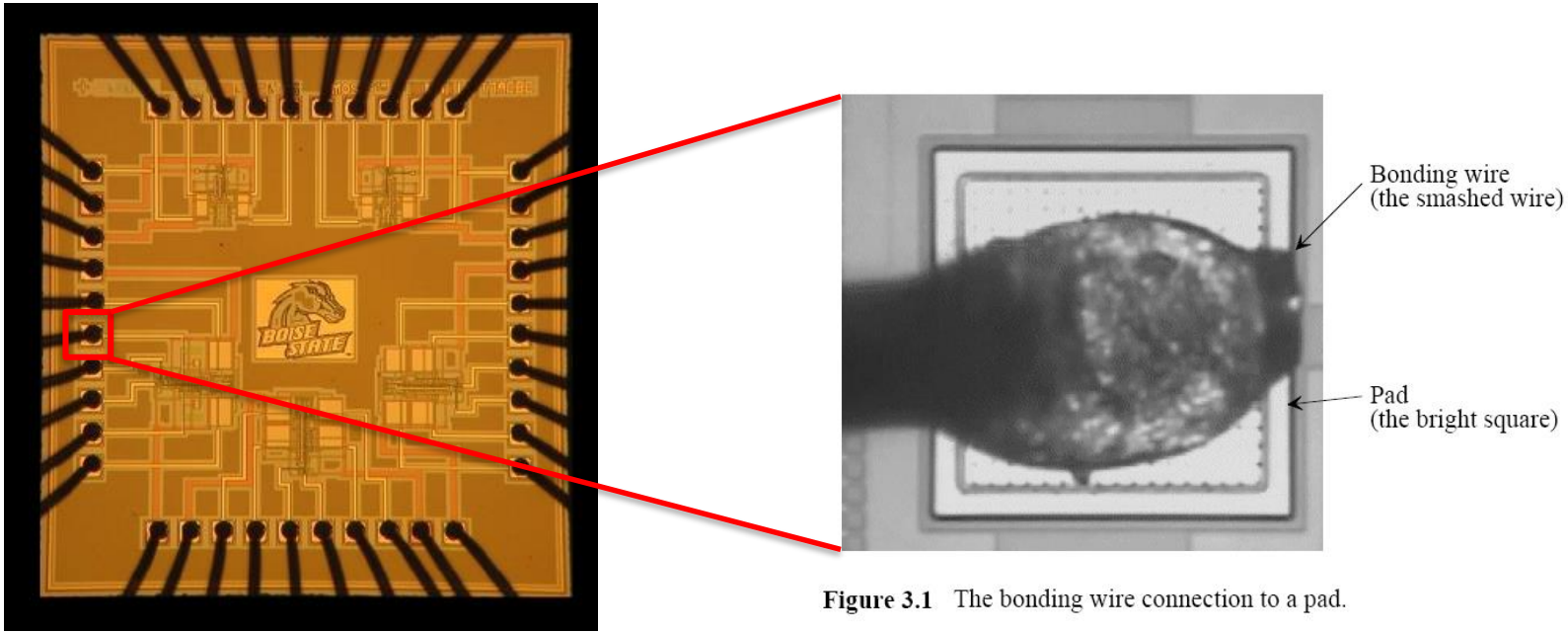

Figure 3.1 The bonding wire connection to a pad.

BOND PAD – CROSS SECTION

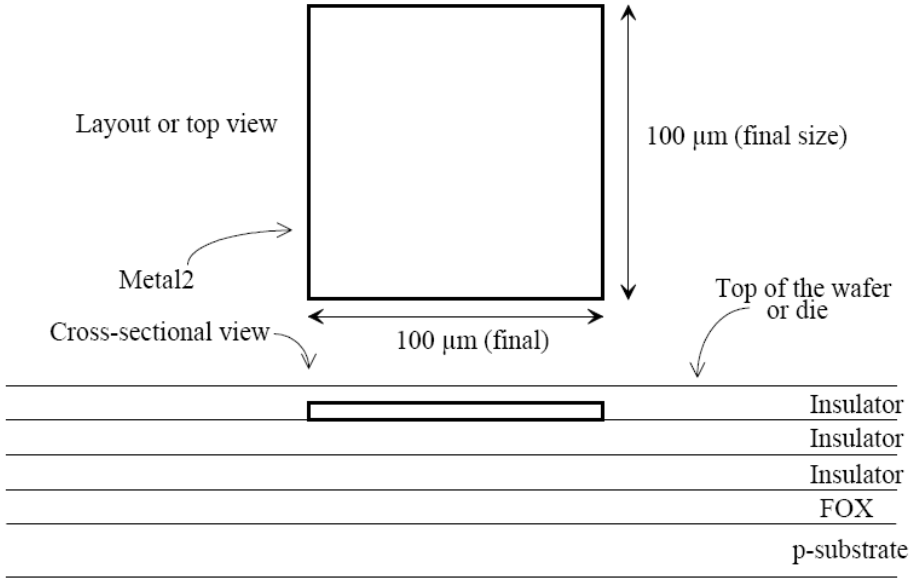

Figure 3.2 Layout of metal2 used for bonding pad with associated cross-sectional view.

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BOND PAD – PASSIVATION OPENING

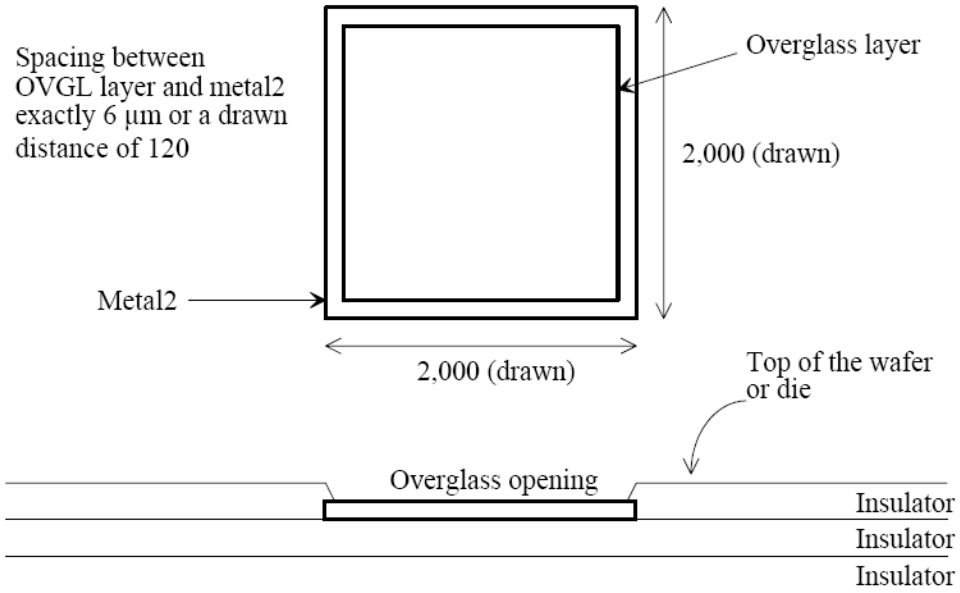

Figure 3.3 Layout of a metal2 pad with pad opening for bonding connection in a 50 nm (scale factor) CMOS process.

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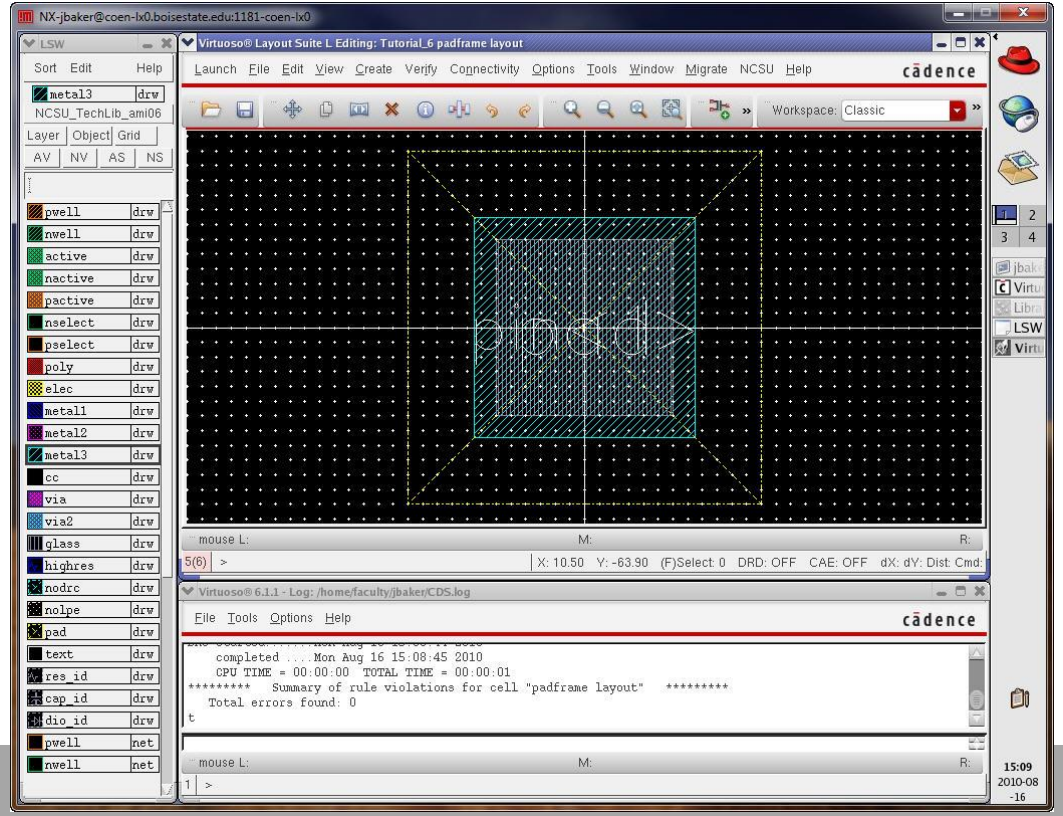
BOND PAD IN C5 PROCESS



- On Semi C5 has three metal layers
- Use top metal (*metal3*) for layout
- *glass* layer defines the passivation opening

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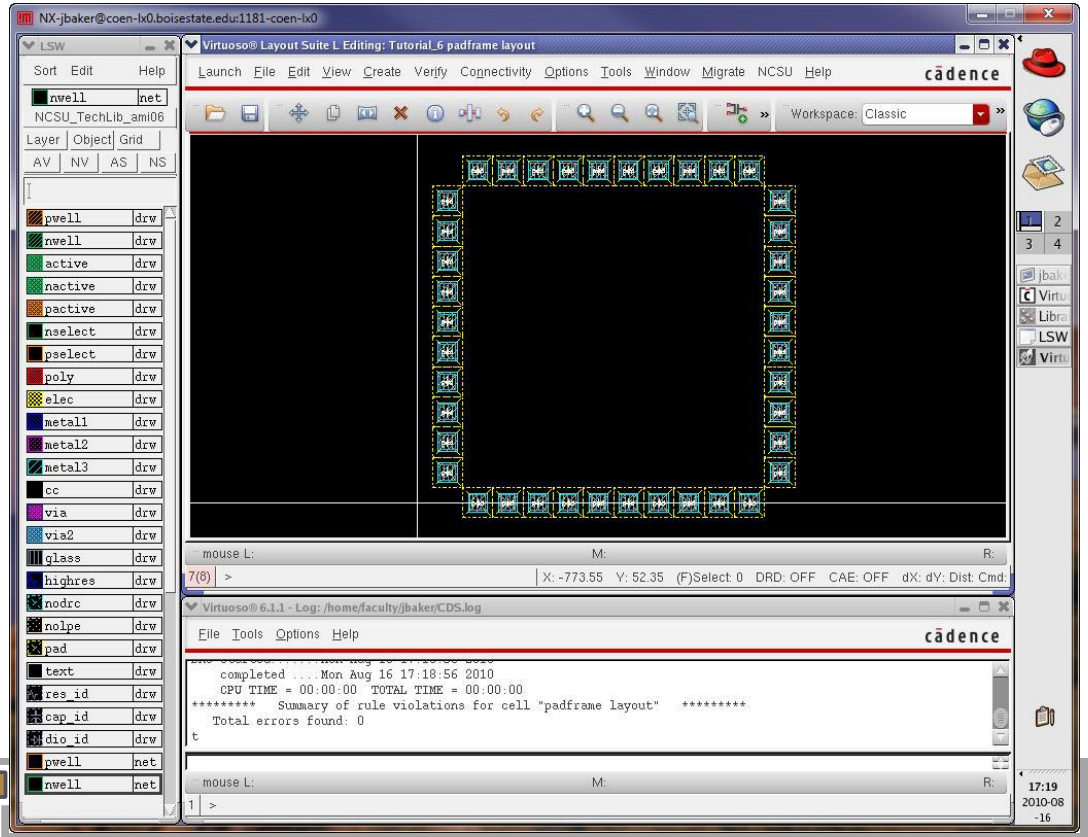
PAD FRAME



- Use array of the bond pad cell to create a pad frame
- In practice ESD protection circuits are required at each I/O
  - Analog and Digital I/O library

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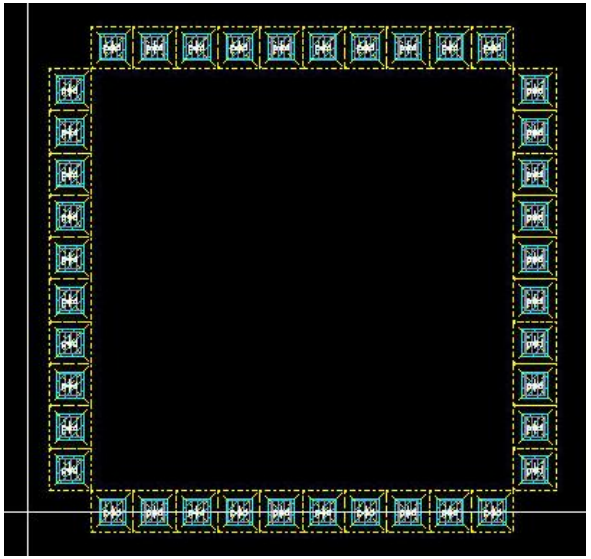
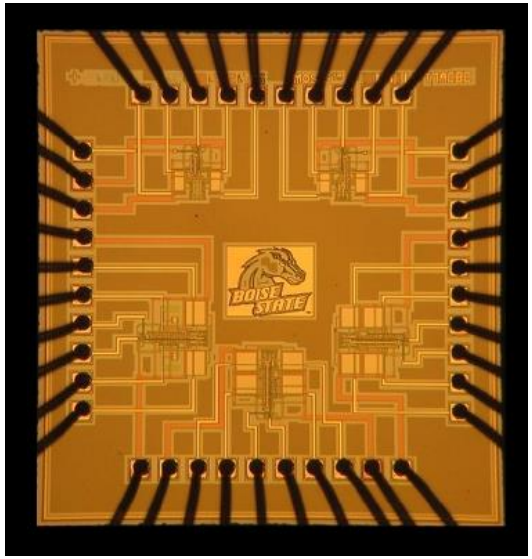
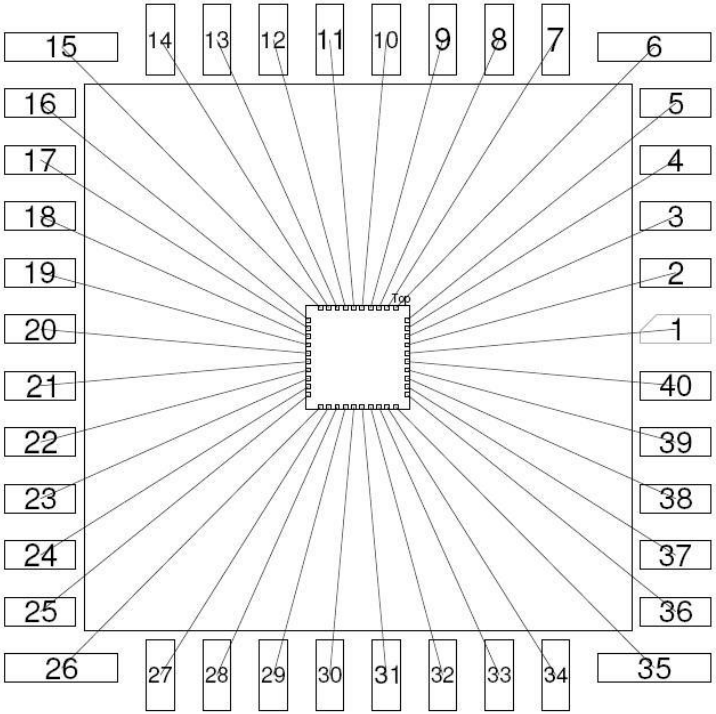
PAD FRAME

- 40-pin pad frame with chip micrograph





BONDING DIAGRAM



- MOSIS creates a bonding diagram
- Define the connections between the chip bonds and the package pins

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