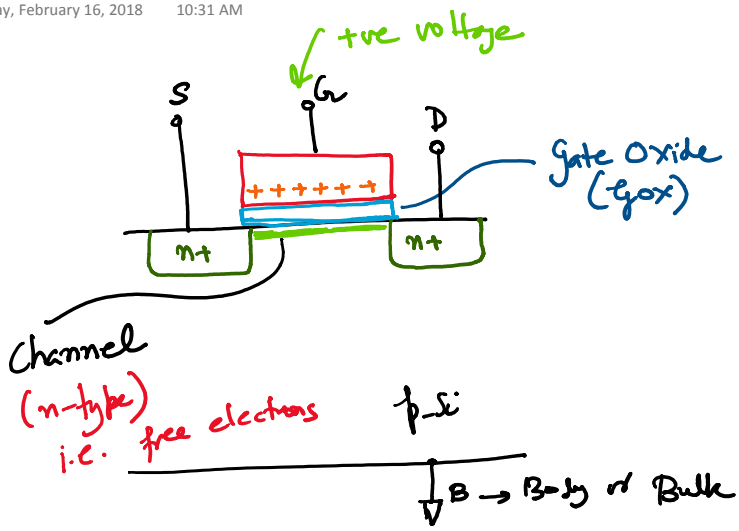
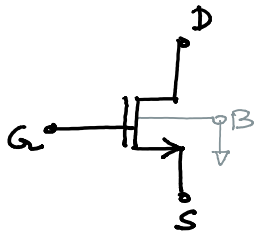
ECE 310 - Lecture 15

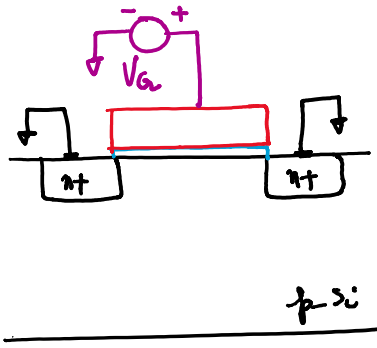
Friday, February 16, 2018 10:31 AM

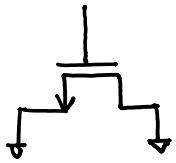
n-channel MOSFET ≡ nFET NMOS





Current always flows from Drain to Source

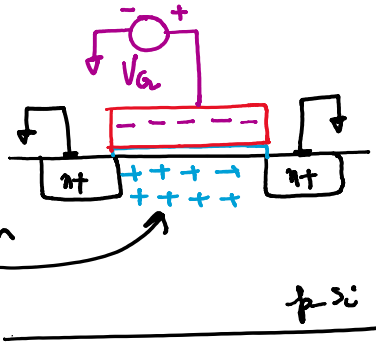




Symbol View

Cross-section view

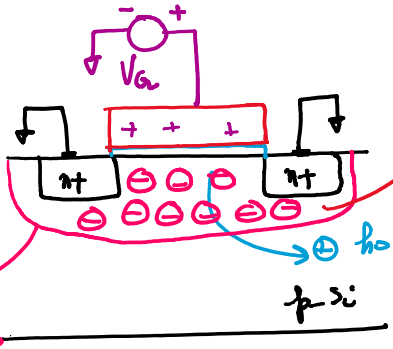
a) $V_G \ll 0$ ← large negative voltage — Accumulation



Accumulation of holes

"Depletion"

b) $V_G \gtrsim 0$ ⇒ slightly larger than zero



-ve charged fixed atoms

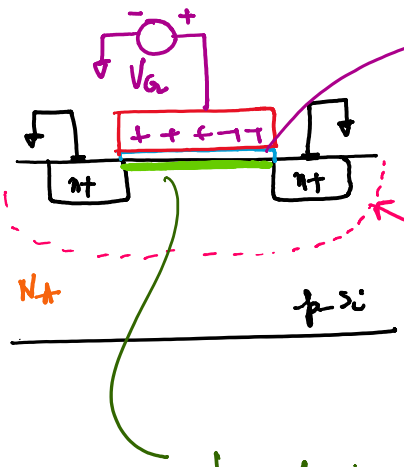
⊕ holes are flushed out

Depletion Region (no carriers left in this region)

c) $V_G > V_{THN}$ ← Threshold Voltage

"INVERSION"

Inversion of the channel region



gate oxide thickness (t_{ox})

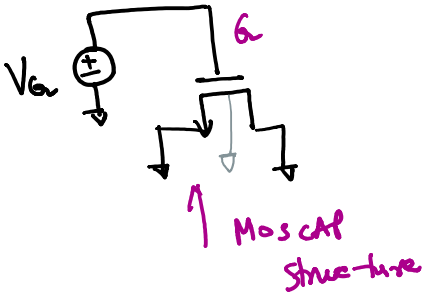
Inversion of the channel region

Depletion Region

$V_{THN} \simeq$ 300mV – 500mV

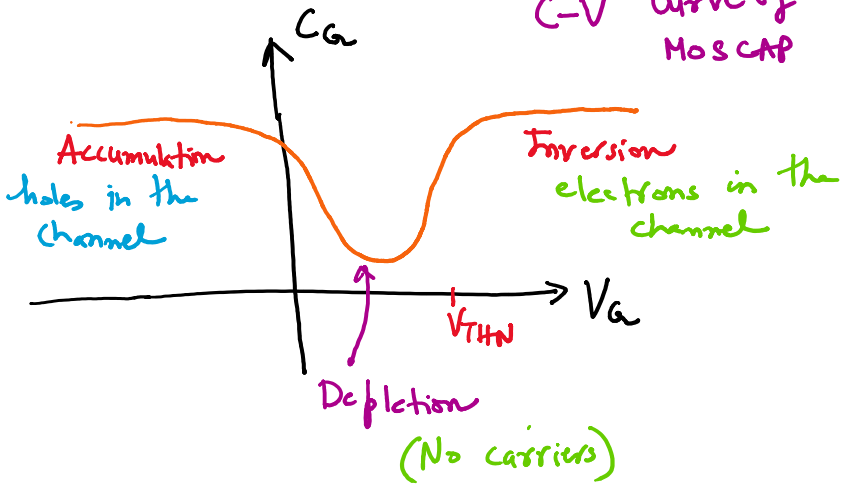
↳ really depends upon Technology used.

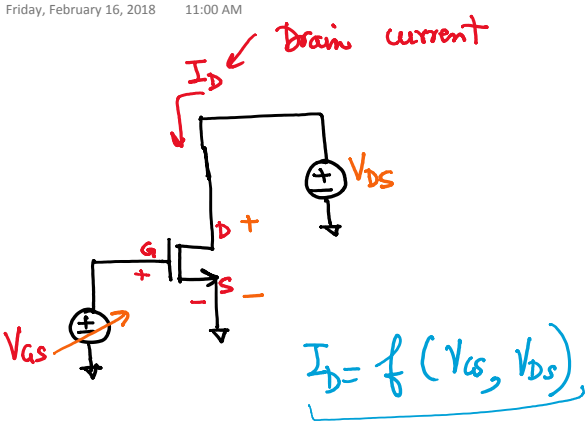
channel is created by inverting the surface.

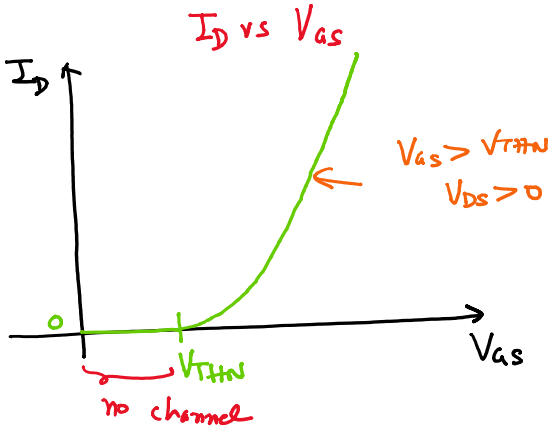


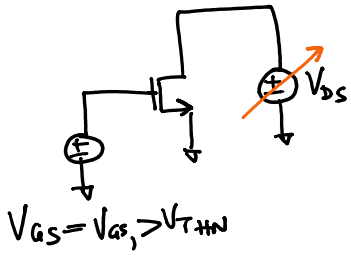
MOSCAP structure

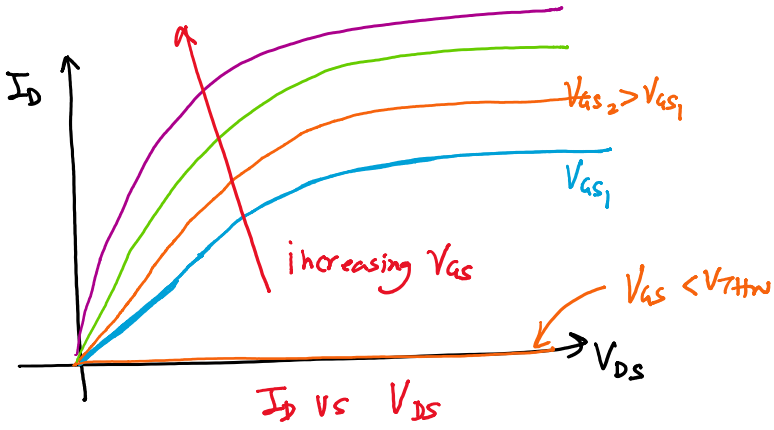
C-V curve of MOSCAP





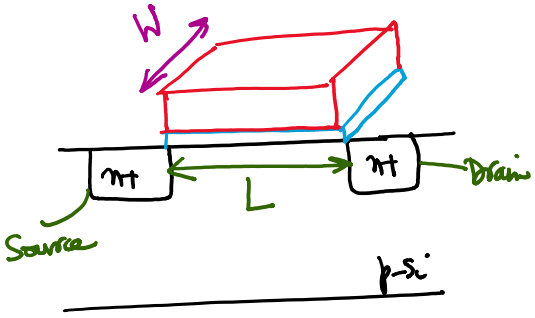






Carrier Transport Mechanism → Drift

↳ electrons are drifted across the channel



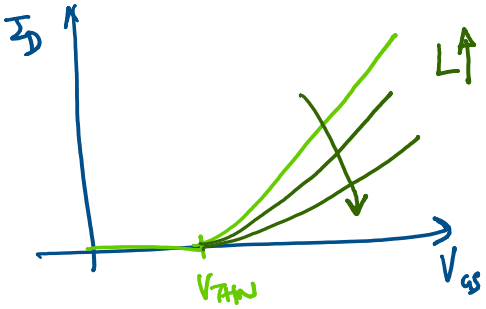
$L \equiv$ Length of MOSFET

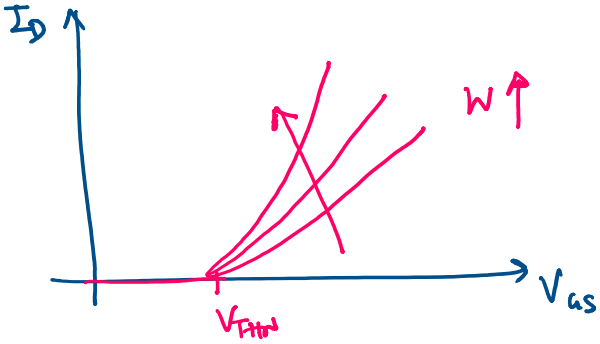
$L \equiv$ 10μm in 1975

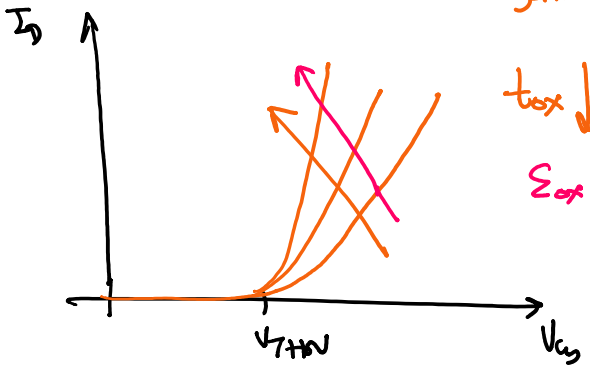
$\backsim$ 10nm in iPhone 8 (2018)

$W \equiv$ Width of the MOSFET

IC designer controls W & L



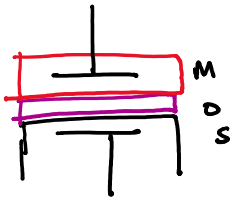




Gate oxide thickness

t_{ox} ↓

ε_{ox} ↑



$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} WL$$

Area

higher oxide capacitance

$\Rightarrow Q = C_{ox} V_G$

$\Rightarrow$ higher charge density

$\hookrightarrow$ larger current

Designers control $\Rightarrow$ W & L, V_{GS}, V_{DS}

Fault control $\Rightarrow$ t_{ox}, ε_{ox}, Doping levels,

Designs

V_{th} control ⇒ t_{ox}, ε_{ox}, Doping levels, mobility etc.