

ECE 310 – MICROELECTRONICS I

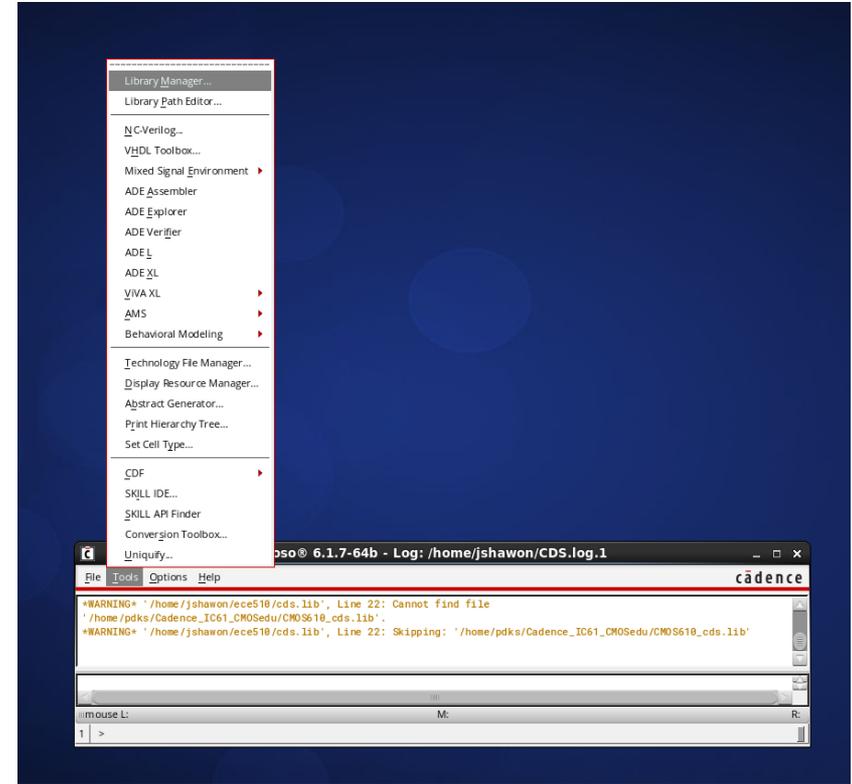
CADENCE TUTORIAL: I-V AND PARAMETRIC SWEEPS

VISHAL SAXENA



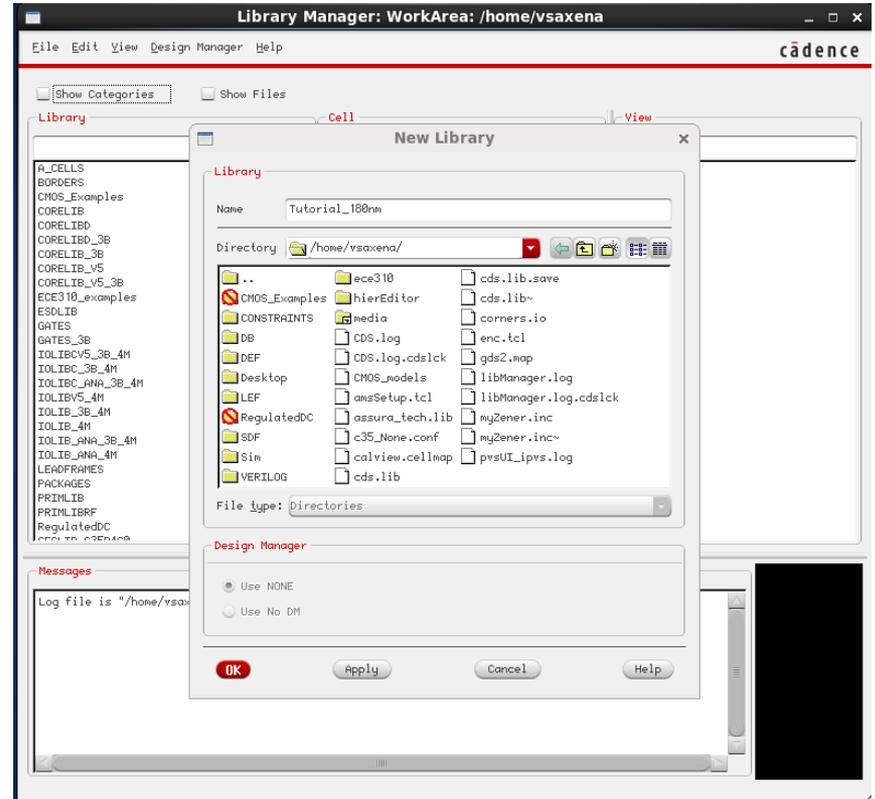
I_D VS V_{GS} (0.18 UM PROCESS)

- Launch Cadence Virtuoso
 - cadsetup ams035
 - virtuoso
- Click on library Manager



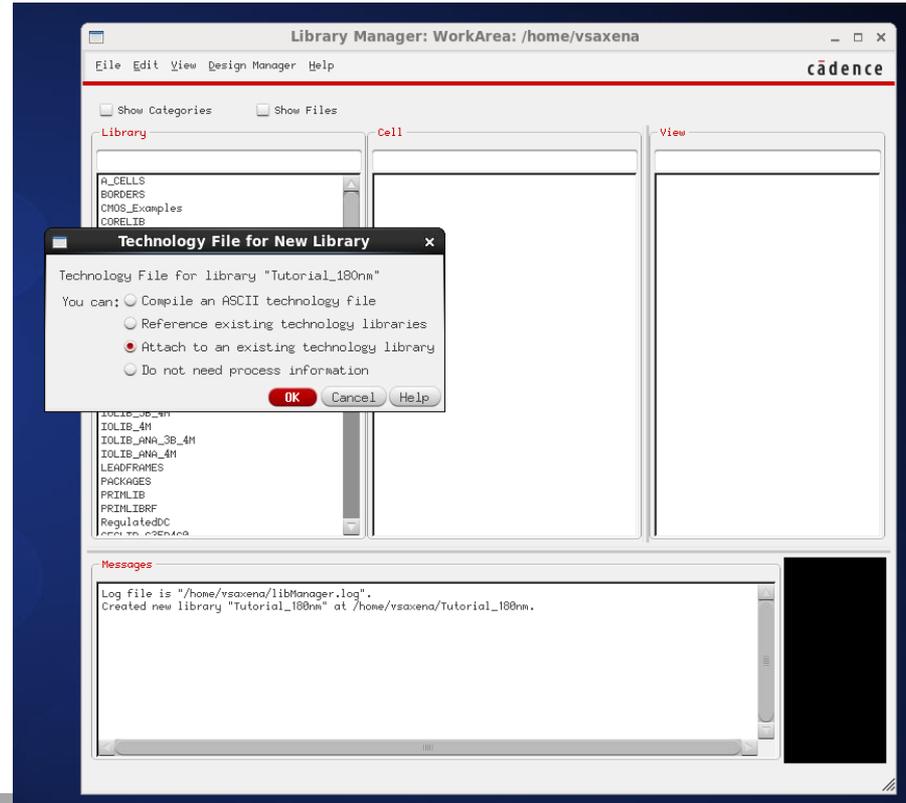
I_D VS V_{GS} (0.18 UM PROCESS)

- Create a new library, say Tutorial_180nm



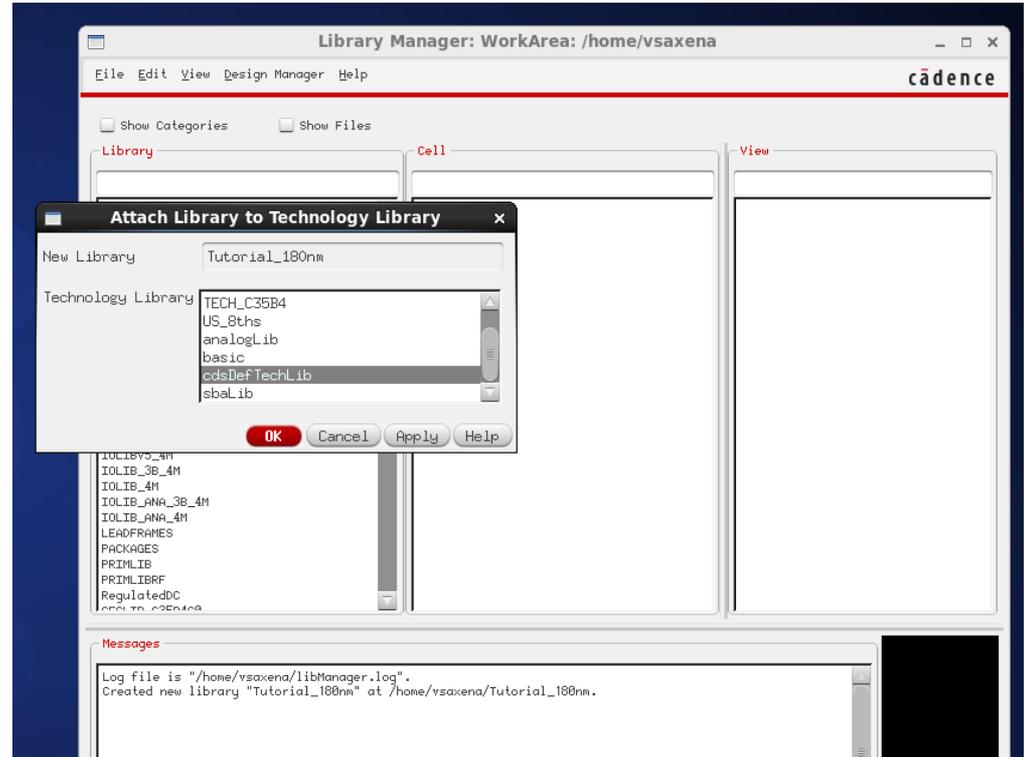
I_D VS V_{GS} (0.18 UM PROCESS)

- Attach it to an existing technology library



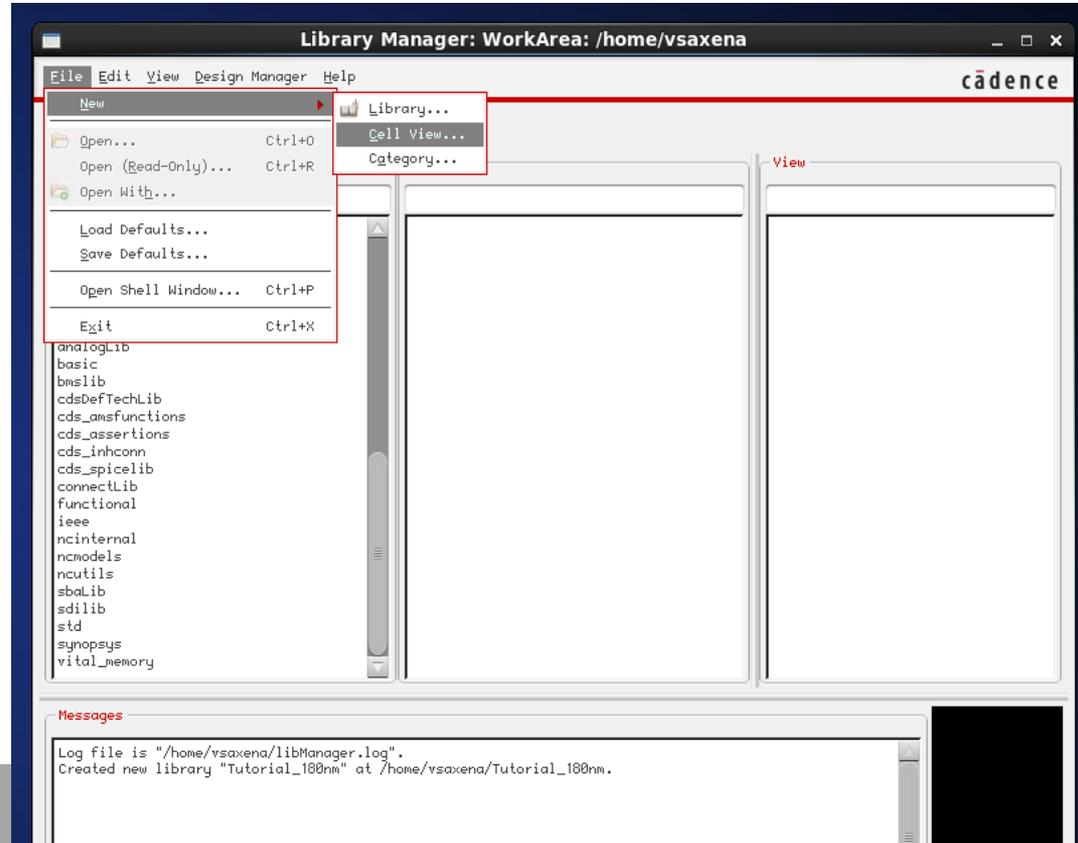
I_D VS V_{GS} (0.18 UM PROCESS)

- In our case it is: "cdsDefTechLib"



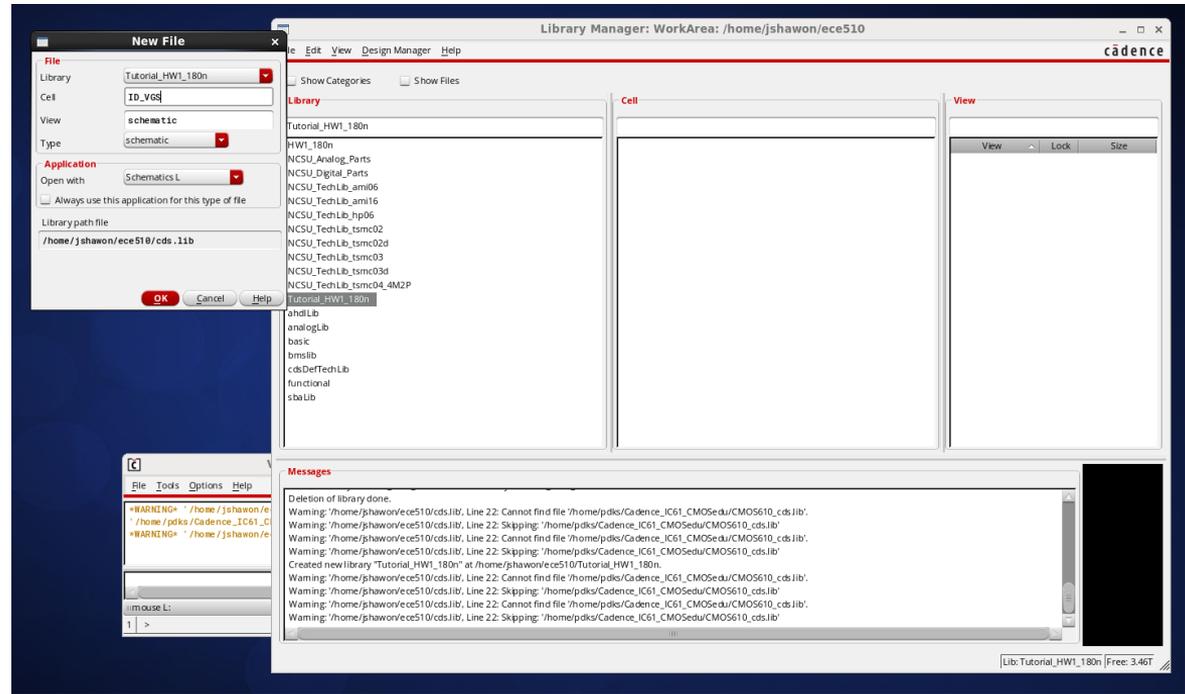
I_D VS V_{GS} (0.18 UM PROCESS)

- Create a cell view



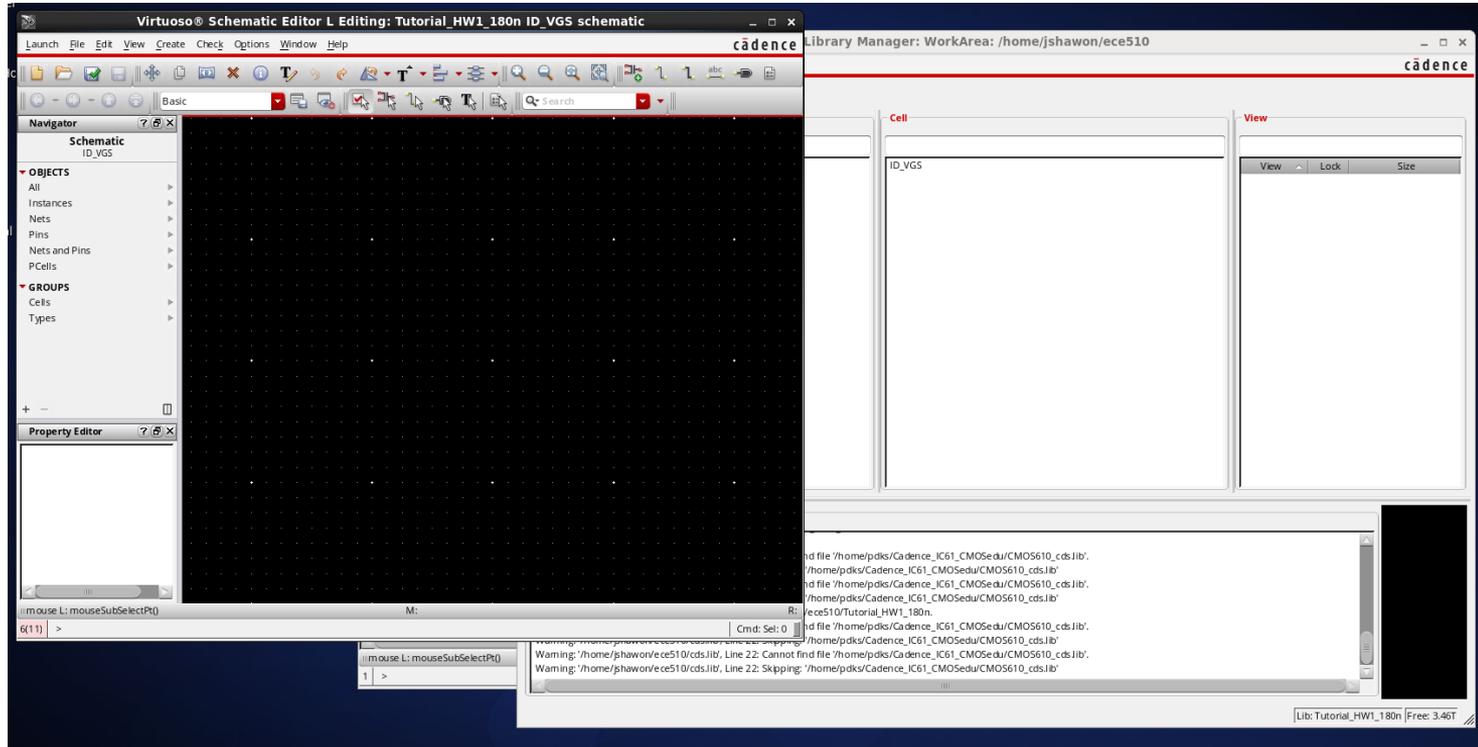
I_D VS V_{GS} (0.18 UM PROCESS)

- Give it an appropriate name. Click OK.



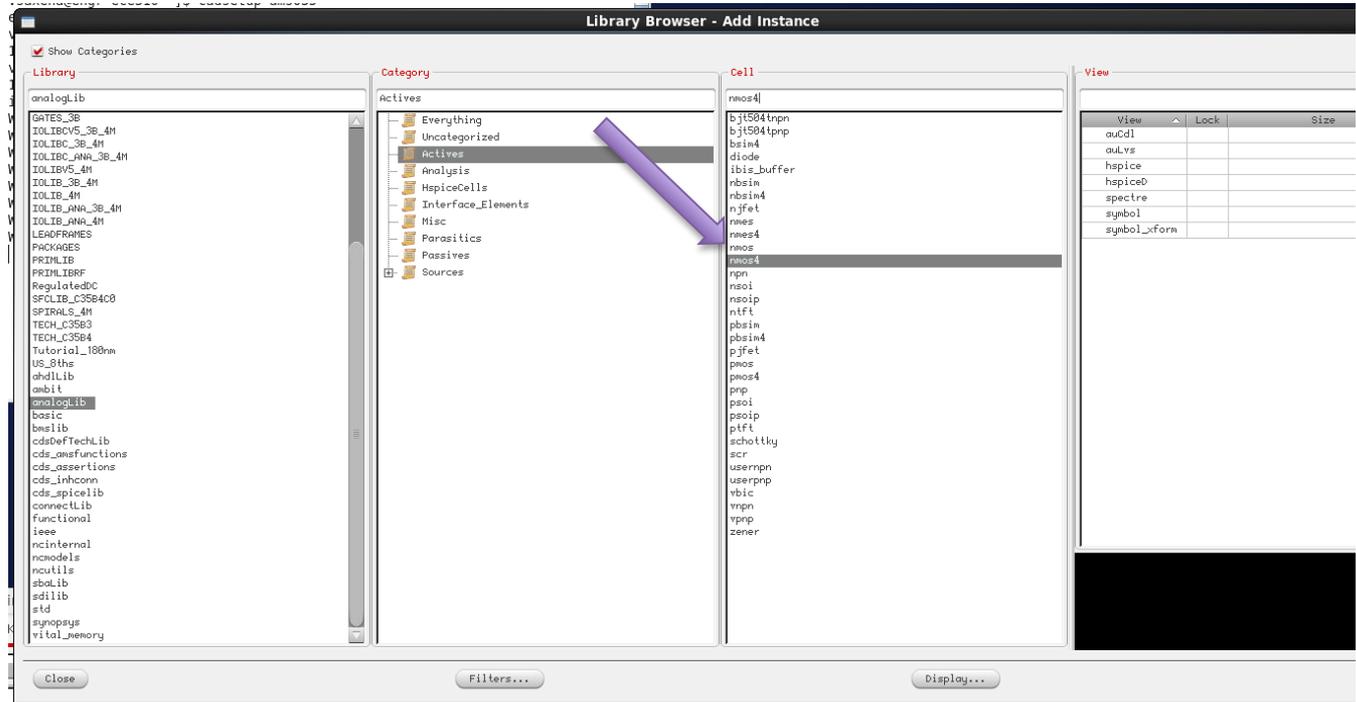
I_D VS V_{GS} (0.18 UM PROCESS)

- The schematic window will pop up.



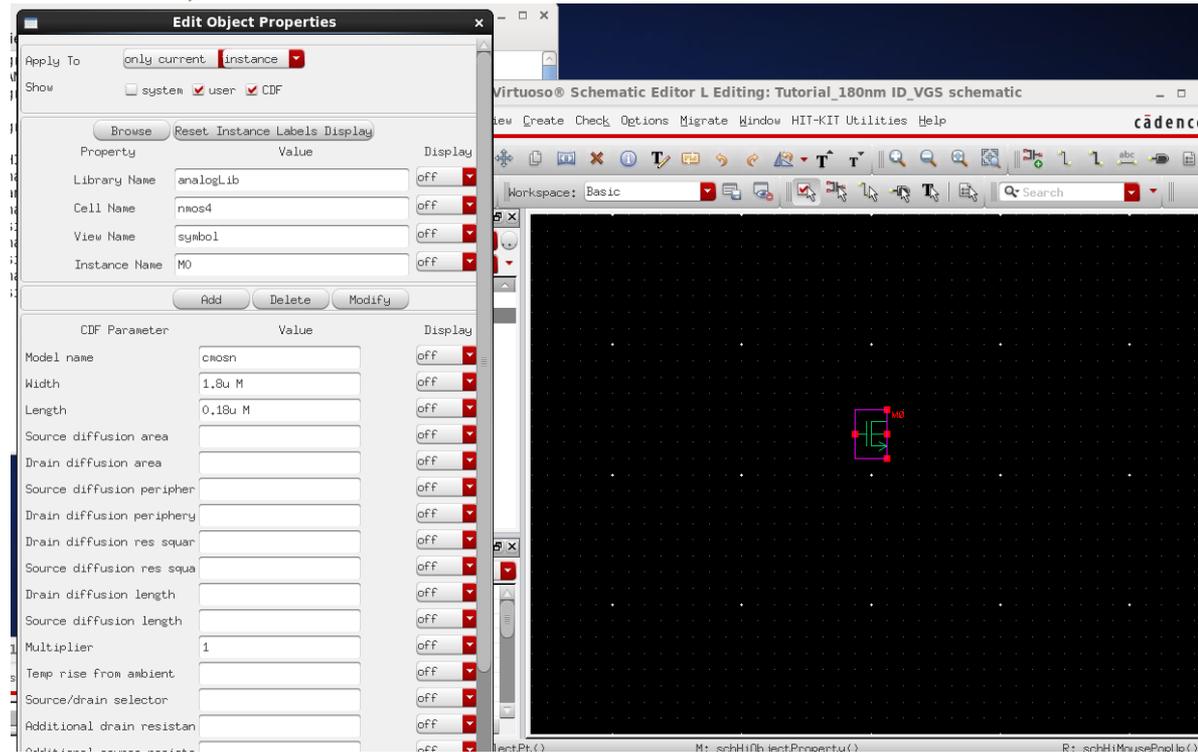
I_D VS V_{GS} (0.18 UM PROCESS)

- Press “I” or click on ‘add instance’ button to add circuit components to the schematic.



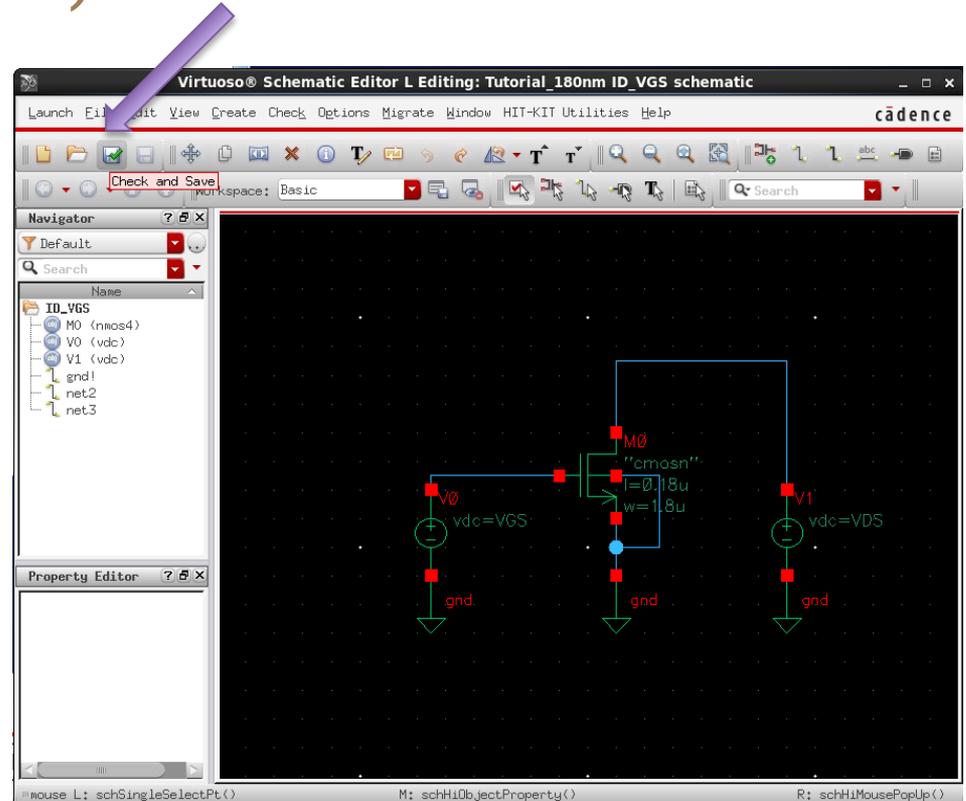
I_D VS V_{GS} (0.18 UM PROCESS)

- From analoglib, select the MOSFET & press “Q” to edit its properties.
- Enter the parameters as shown in the screenshot.
- Don’t forget to put the model name “**cmosn**” for NMOS and “**cmosp**” for PMOS.
- Also, **always use absolute size of the MOSFET (0.18u NOT 0.18)**



I_D VS V_{GS} (0.18 UM PROCESS)

- Complete the schematic
- Click on the “check and Save” Button to check if there is any error present in this schematic.
- Debug and fix any errors in the schematic.



I_D VS V_{GS} (0.18 UM PROCESS)

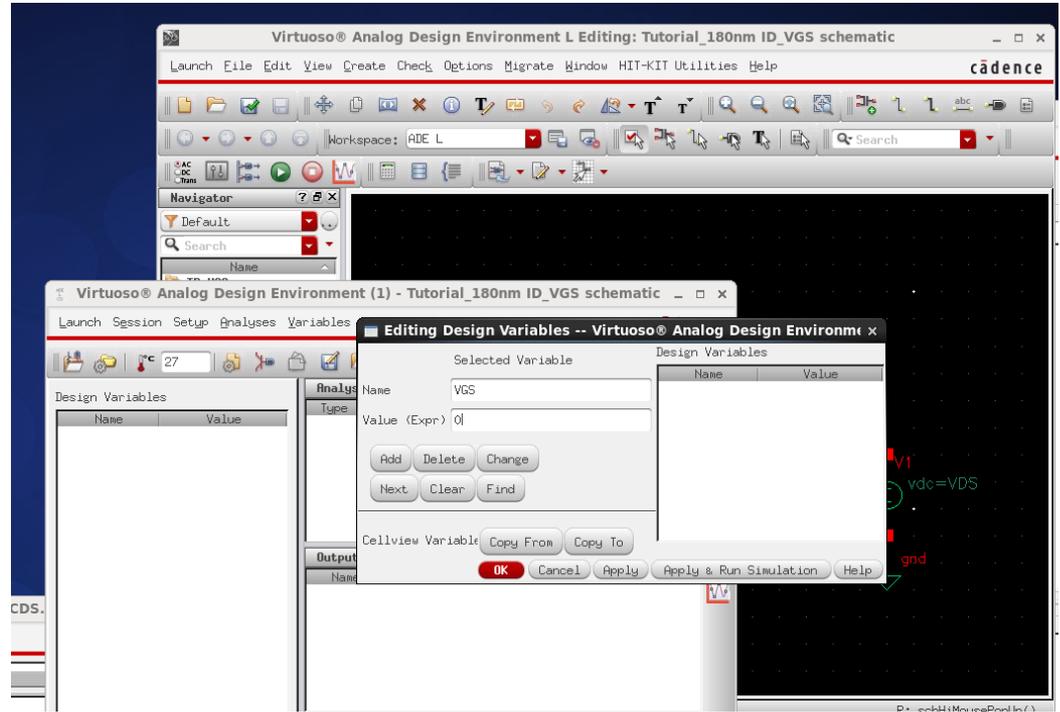
- Launch ADE L to simulate the circuit.
- Add variables for simulation.

The image shows two overlapping windows from the Cadence Virtuoso Analog Design Environment L. The top window, titled "Virtuoso® Analog Design Environment L Editing: Tutorial_180nm ID_VGS schematic", displays a menu with options: Launch, File, Edit, View, Create, Check, Options, Migrate, Window, HIT-KIT Utilities, and Help. Below the menu is a toolbar and a search bar. The bottom window, titled "Virtuoso® Analog Design Environment (1) - Tutorial_180nm ID_VGS schematic", shows the "Variables" dialog box. The dialog has tabs for "Variables" and "Outputs". The "Variables" tab is active, showing a table with columns "Name" and "Value". A context menu is open over the "Variables" tab, listing options: Edit..., Delete, Find, Copy From Cellview, and Copy To Cellview. The "Outputs" tab is also visible, showing a table with columns "Name/Signal/Expr", "Value", "Plot", "Save", and "Save Options". In the background, a circuit schematic is visible, featuring a MOSFET model with parameters: $\tau_{mosn} = 0.18u$ and $\eta = 1.8u$. The gate is connected to a voltage source $V1$ with $vdc = VDS$, and the source is connected to ground (gnd).



I_D VS V_{GS} (0.18 UM PROCESS)

- Click “add” and “OK” (both VDS & VGS; select appropriate values for them)



I_D VS V_{GS} (0.18 UM PROCESS)

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic with a MOSFET model and a voltage source. The voltage source is labeled 'v1' and has a value of 'vdc=VDS'. The MOSFET model is labeled 'm0' and has parameters 'l=0.18u' and 'w=1.8u'. The schematic is connected to ground ('gnd').

Overlaid on the schematic are two windows:

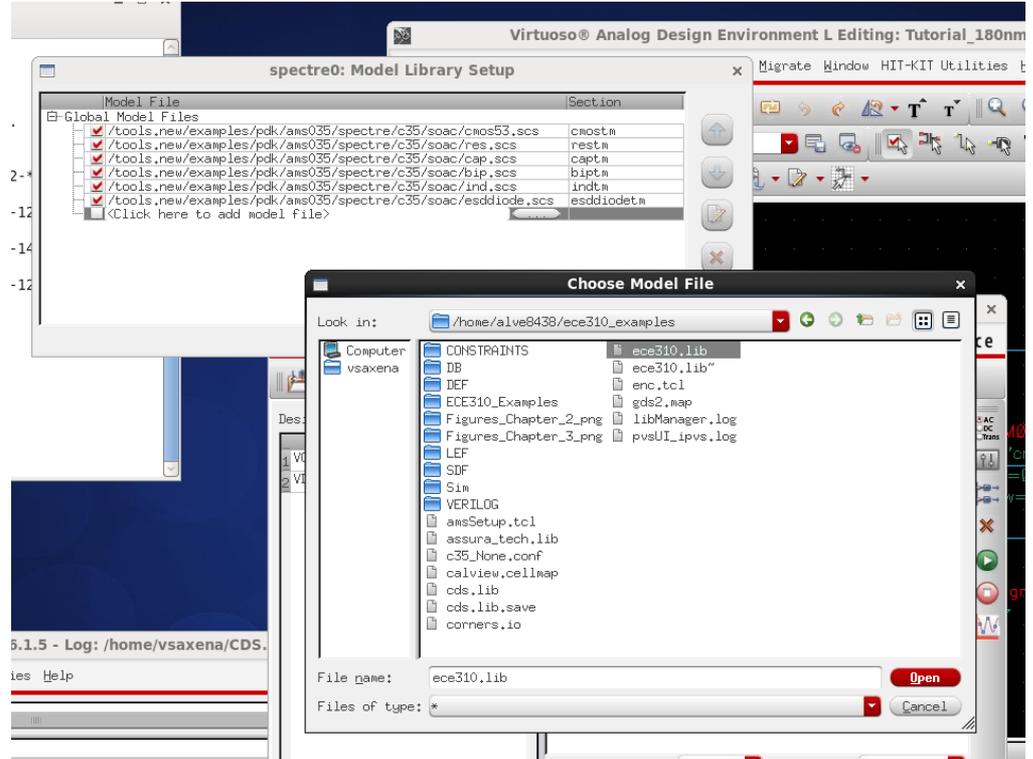
- Design Variables:** A table with two rows:

Name	Value
1 VGS	0
2 VDS	0
- Analyses:** A table with columns 'Type', 'Enable', and 'Arguments'. It is currently empty.
- Outputs:** A table with columns 'Name/Signal/Expr', 'Value', 'Plot', 'Save', and 'Save Options'. It is currently empty.



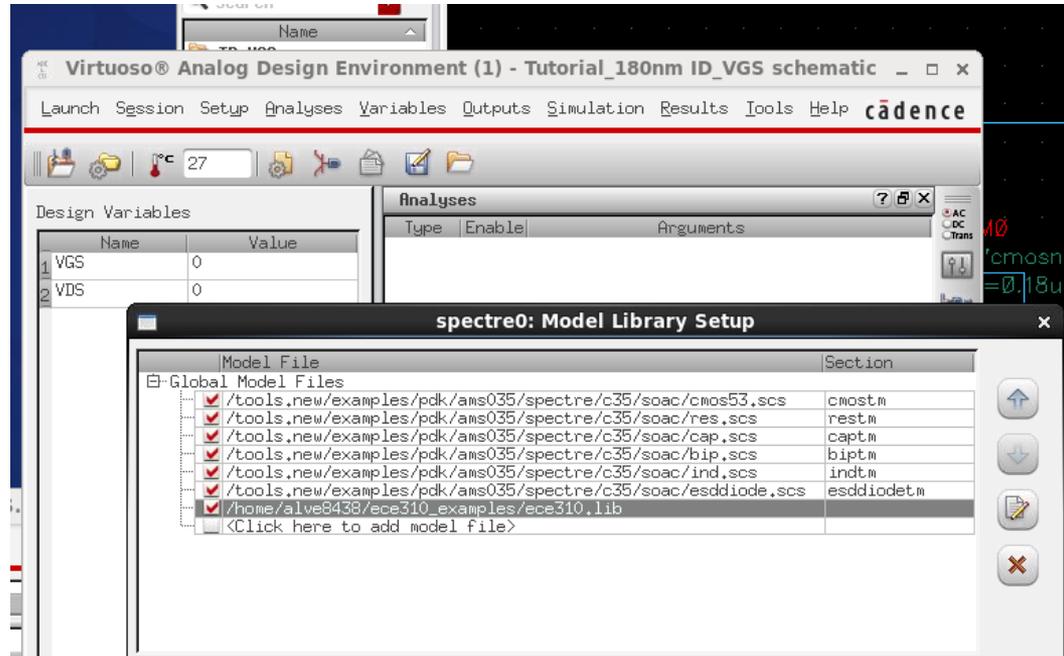
I_D VS V_{GS} (0.18 UM PROCESS)

- Now, we have to link the model parameters to our device. Therefore, click:
Setup->Model Libraries
- Browse for the model file and add to the list



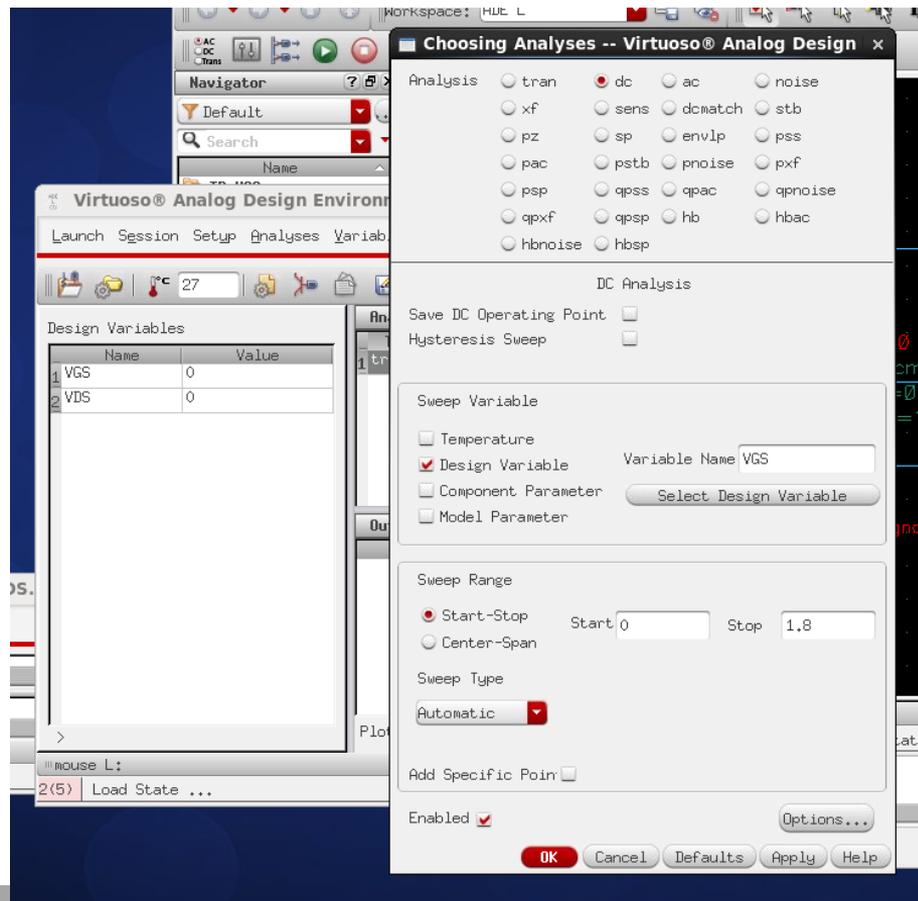
I_D VS V_{GS} (0.18 UM PROCESS)

- For ECE310, models are located at:
/home/alve8438/ece310_examples/ece310.lib



I_D VS V_{GS} (0.18 UM PROCESS)

- Setup DC analysis to sweep the required voltages



I_D VS V_{GS} (0.18 UM PROCESS)

- Select the outputs to be plotted from the schematic
- **Outputs->To be Plotted->Select On Schematic**

The screenshot displays the Cadence Virtuoso Analog Design Environment (ADE L) interface. The main window shows a schematic of a MOSFET circuit with a gate terminal labeled V_{GS} and a drain terminal labeled V_1 with $vdc=VDS$. The circuit parameters are $T=0.18\mu$ and $w=1.8\mu$. The interface includes several panels:

- Design Variables:** A table with columns Name and Value.
- Analyses:** A table with columns Type, Enable, and Arguments.
- Outputs:** A table with columns Name/Signal/Expr, Value, Plot, Save, and Save Options.

Name	Value
VGS	0
VDS	0

Type	Enable	Arguments
dc	<input checked="" type="checkbox"/>	0 1.8 Automatic Start-Stop

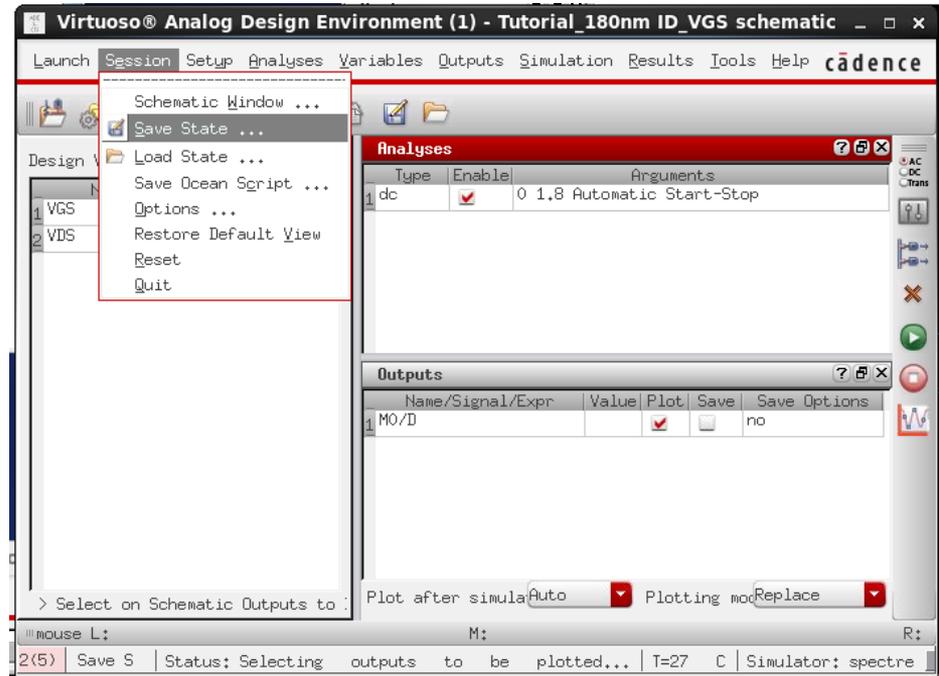
Name/Signal/Expr	Value	Plot	Save	Save Options
M0/D		<input checked="" type="checkbox"/>	<input type="checkbox"/>	no

At the bottom of the interface, the status bar shows the command: `Plot after simulation auto` and `Plotting mode Replace`.



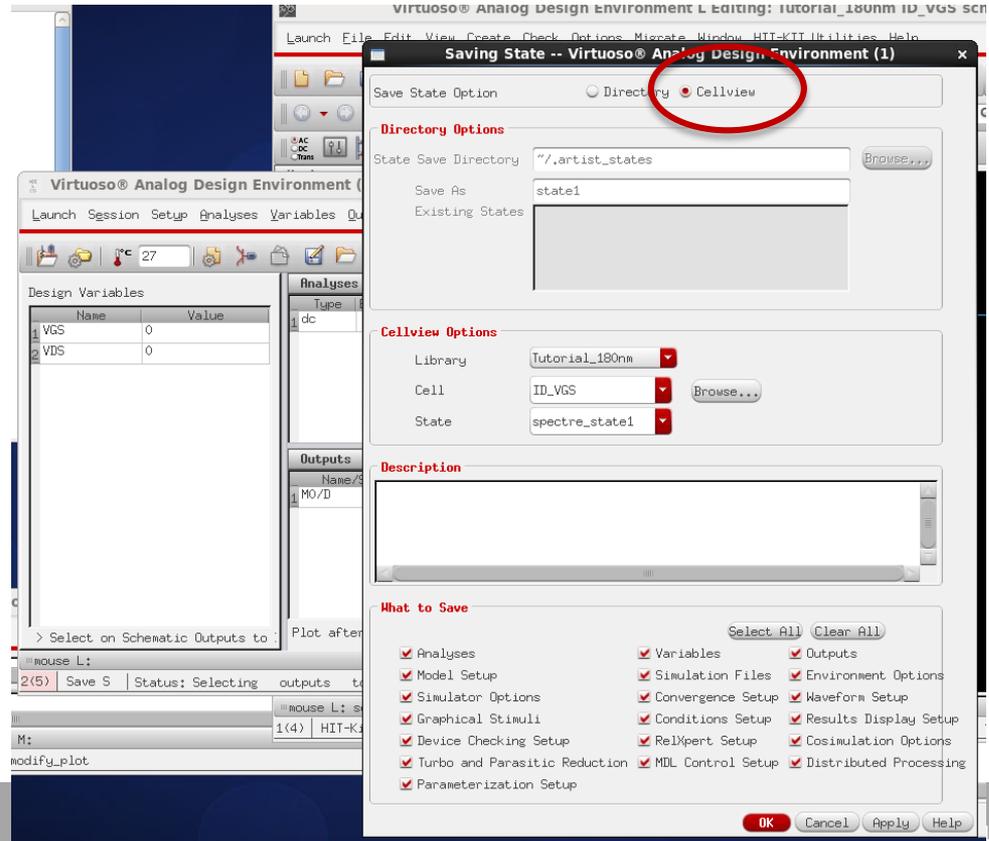
I_D VS V_{GS} (0.18 UM PROCESS)

- Save the state



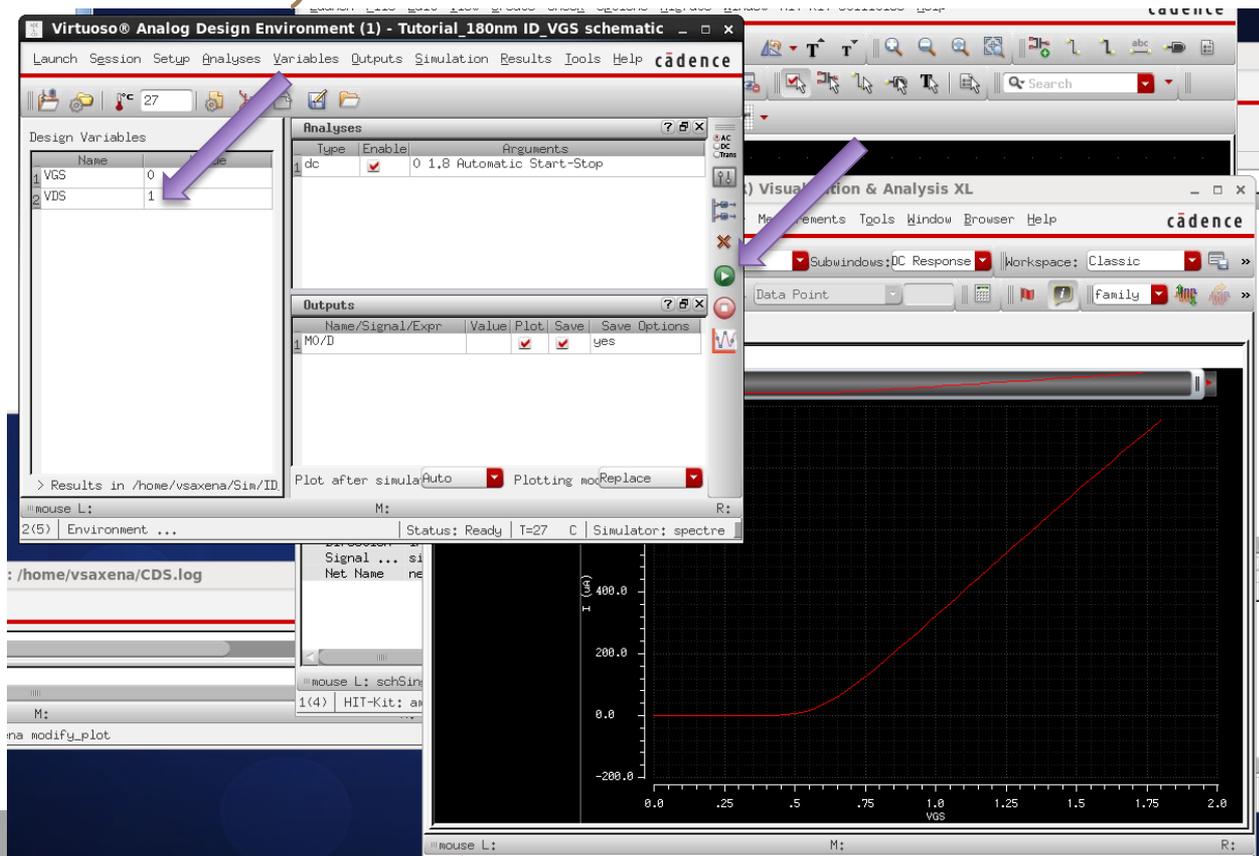
I_D VS V_{GS} (0.18 UM PROCESS)

- Always save the state in the **Cellview**



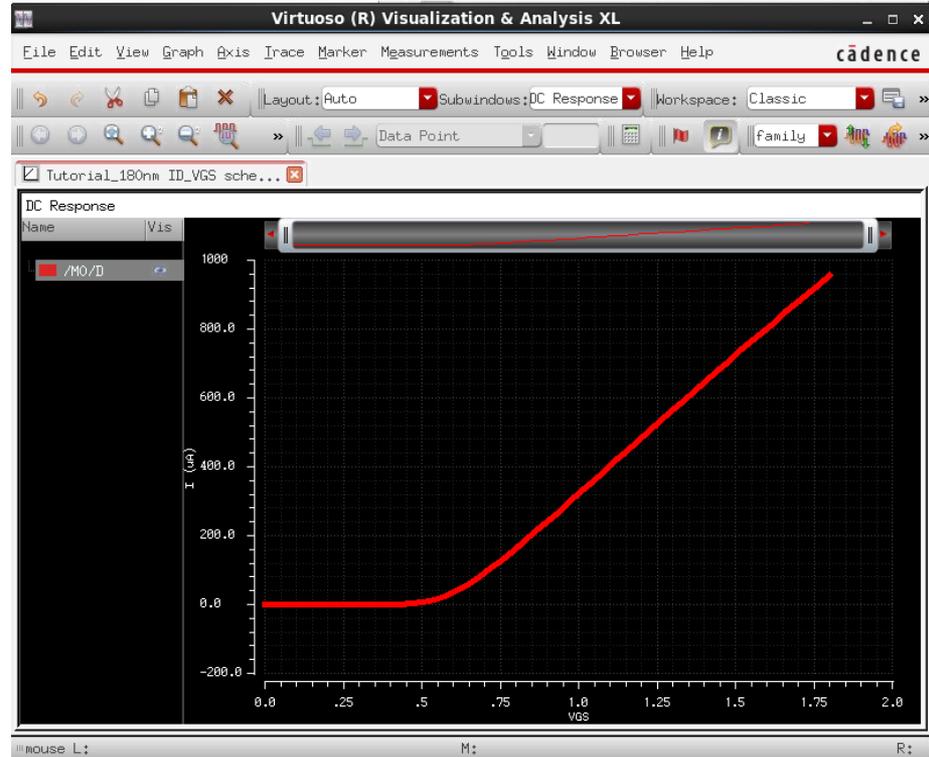
I_D VS V_{GS} (0.18 UM PROCESS)

- Now, for this particular analysis, we have to select a value for VDS. Here, we have set it as 1V.
- Click “Netlist and Run”



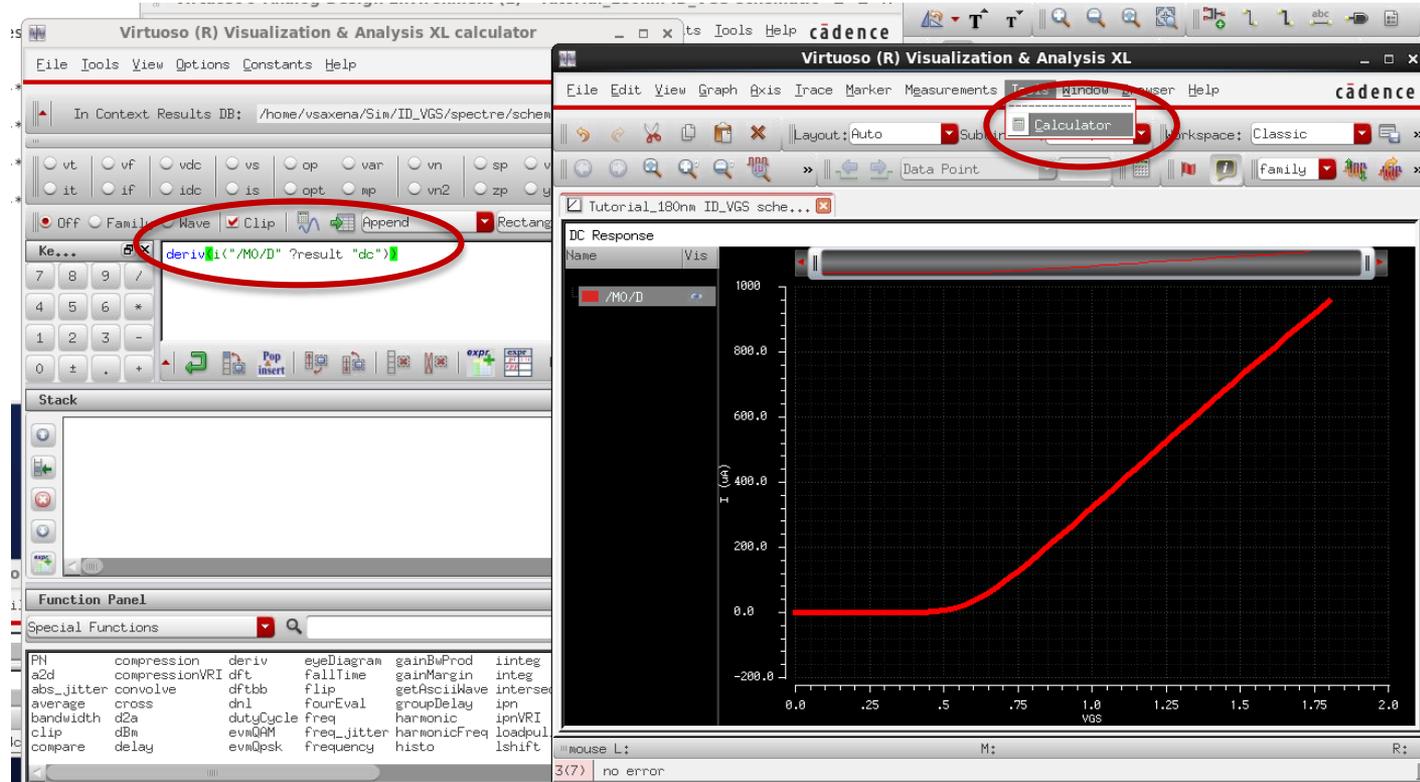
I_D VS V_{GS} (0.18 UM PROCESS)

- I_D vs V_{GS} Plot



PLOTTING g_m

- To plot g_m , use calculator from Tools menu
- `deriv()` operator provides the derivative



PLOTTING GM

The screenshot displays the Virtuoso (R) Visualization & Analysis XL calculator interface. The main window shows a plot of Gain Margin (GM) versus VGS. The plot has two y-axes, both ranging from -200.0 to 1000.0. The x-axis ranges from 0.0 to 2.0. A red curve represents the Gain Margin, which starts at 0.0 dB at 0.0 VGS and increases to approximately 800.0 dB at 1.75 VGS. A blue curve represents the phase margin, which starts at 0.0 dB at 0.0 VGS and increases to approximately 800.0 dB at 1.0 VGS, then remains flat. The plot is titled "ID_VGS sche...".

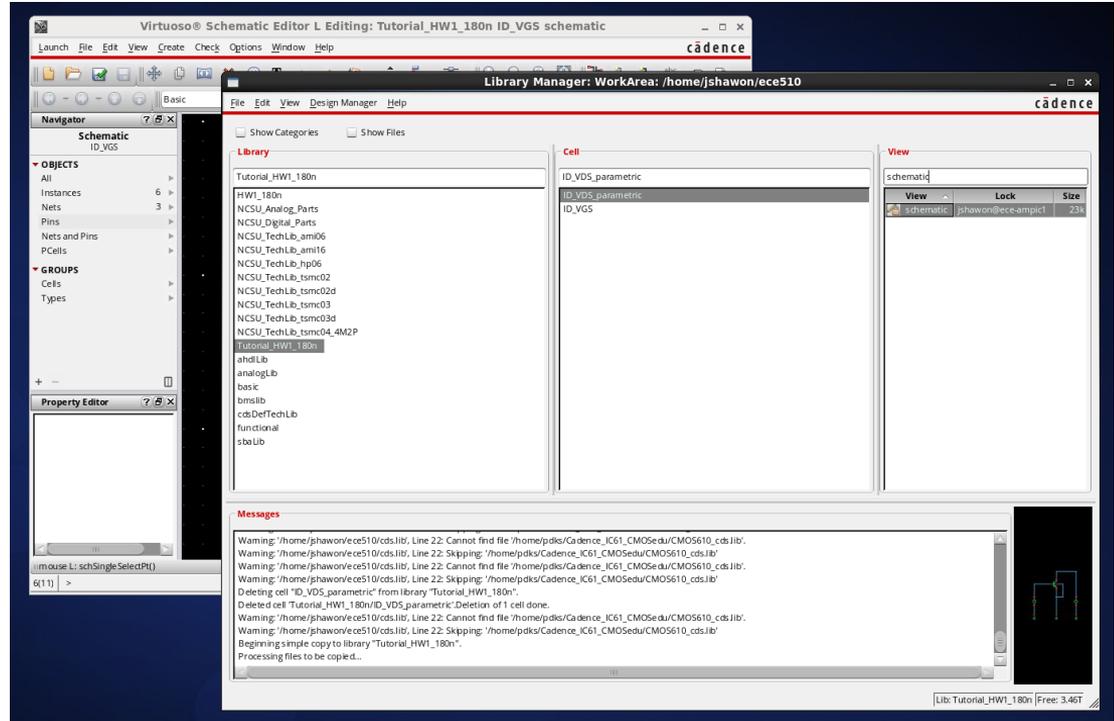
The calculator interface includes a menu bar (File, Tools, View, Options, Constants, Help), a toolbar, and a command line. The command line shows the expression: `deriv.i("M0/D")?re[Evaluate the buffer. If scalar, display in buffer. If waveform, plot]`. The calculator also features a Stack, Function Panel, and a list of Special Functions.

Special Functions						
PN	compression	deriv	eyeDiagram	gainBwProd	iinteg	overshoot
a2d	compressionVRI	dft	fallTime	gainMargin	integ	pavg
abs_jitter	convolve	dftbb	flip	getAsciiWave	intersect	peak
average	cross	dnl	fourEval	groupDelay	ipn	peakToPeak
bandwidth	d2a	dutyCycle	freq	harmonic	ipnVRI	period_jitter
clip	dBm	evmQAM	freq_jitter	harmonicFreq	loadpull	phaseMargin
compare	delay	evmQpsk	frequency	histo	lshift	phaseNoise



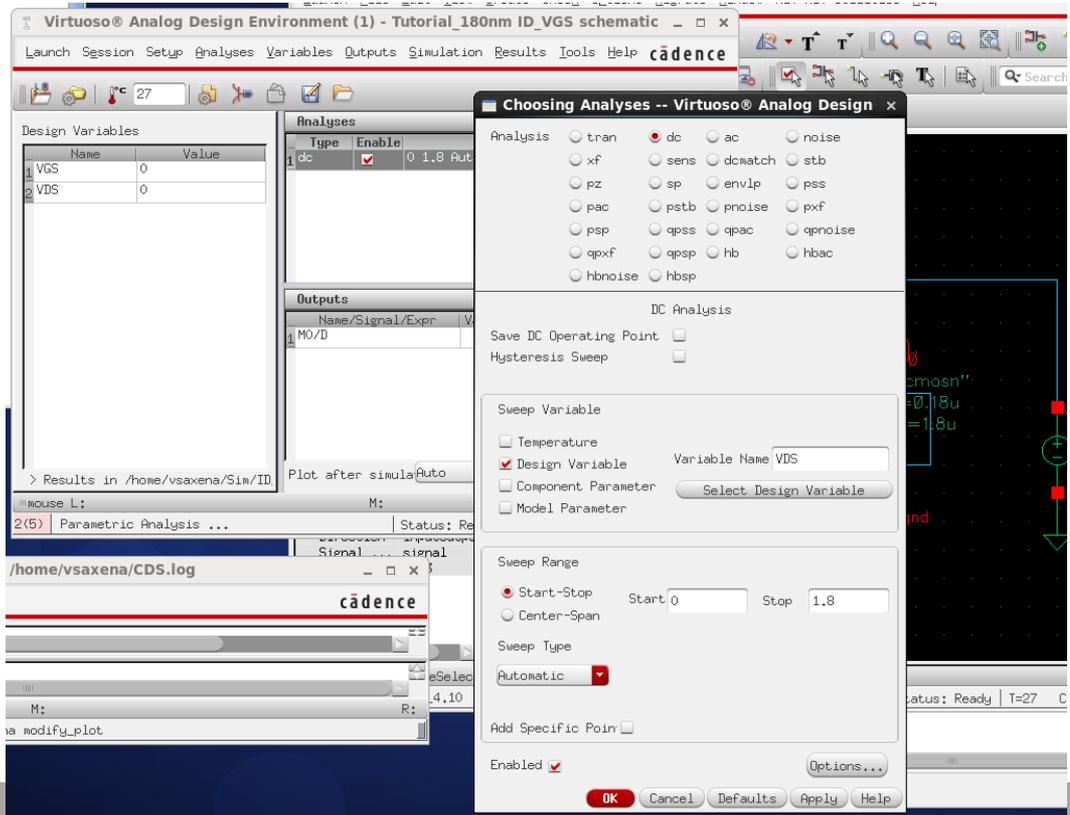
I_D VS V_{DS} FOR DIFFERENT V_{GS} (0.18 UM PROCESS)

- Like before, you may create another cellview for ID-VDS sweep or just use the previous one



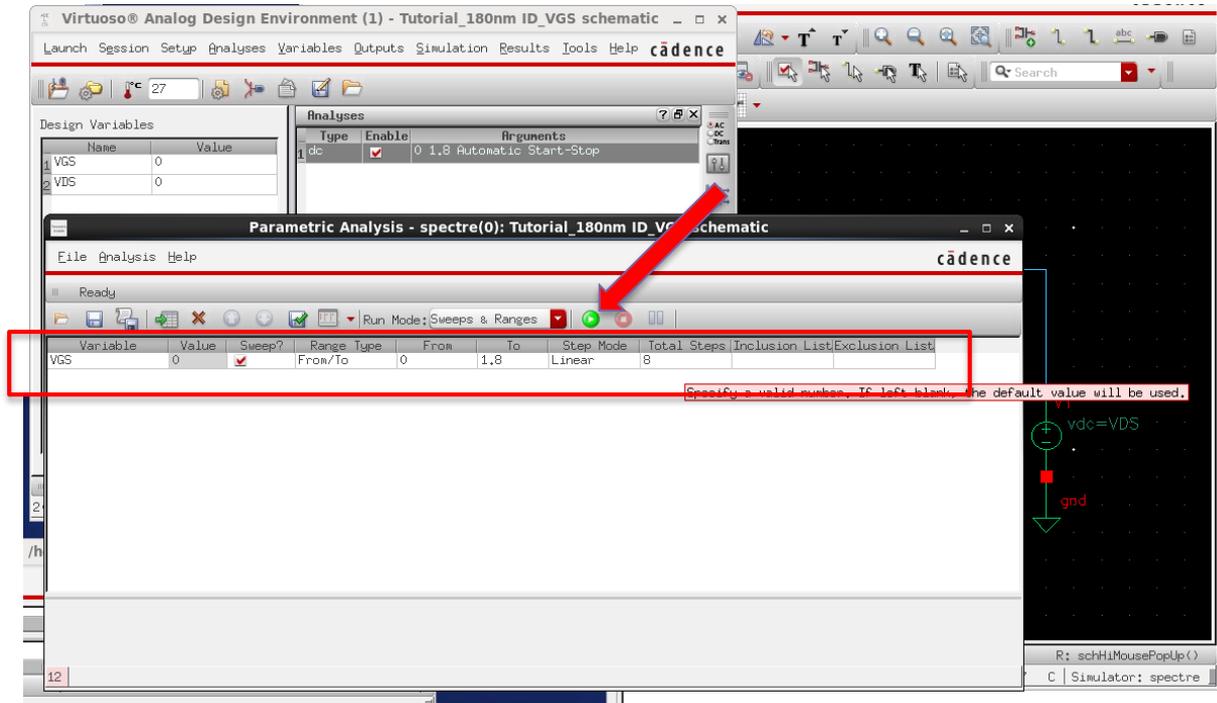
I_D VS V_{DS} FOR DIFFERENT V_{GS} (0.18 UM PROCESS)

- Create a DC sweep analysis for VDS
- This will provide one ID-VDS plot
- But we need a family of curves for varying VGS



I_D VS V_{DS} FOR DIFFERENT V_{GS} (0.18 UM PROCESS)

- For parametric analysis, click:
Tools > Parametric Analysis
- Setup the parametric analysis to double sweep V_{GS} along with V_{DS}
 - Think of it as two nested for loops in a code
- Click on the green button to run the analysis



I_D VS V_{DS} FOR DIFFERENT V_{GS} (0.18 UM PROCESS)



PMOS SIMULATIONS

- Now, figure out how to obtain ID-VSG and ID-VSD plots for the PMOSFETs
- Note that the body of the PMOS should be tied to VDD

