Name: ________________________________

# FINAL EXAM

*Closed book, closed notes. Calculators may be used for numeric computations only. All work is to be your own - **show your work** for maximum partial credit.*

**Data:**
Use the following data in the problems unless otherwise:

***MOSFETs***

| | |
|---|---|
| $V_{DD}$ | 1.8V |
| $\mu_n C_{ox}$ | 200 μA/V$^2$ |
| $\mu_p C_{ox}$ | 100 μA/V$^2$ |
| $V_{THN}$ | 0.4V |
| $\lvert V_{THP}\rvert$ | 0.5V |

***BJTs***

| | |
|---|---|
| $V_{CC}$ | 2.5V |
| $\beta_{npn}$ | 100 |
| $\beta_{pnp}$ | 50 |
| $I_S$ | $8\times10^{-16}$ A |
| $V_{BE,nom}$ | 0.7V |
| $V_A$ | 5V |

**Fundamental Constants**

$$k = 1.38\times10^{-23} \text{ J/K} \quad q = 1.60\times10^{-19} \text{ C}$$

$$v_T = \frac{kT}{q} = 26mV\ @\ 300°K$$

**Semiconductor constants for Si**

$$E_g = 1.12eV \quad n_i(T = 300K) = 1.5\times10^{10}\, cm^{-3}$$

**PN junction Equations**

$$V_{bi} = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad N_A x_p = N_D x_n$$

$$I_D = I_S\left(e^{\frac{V_D}{V_T}} - 1\right)$$

**NMOS Equations**

*Cutoff region*

$$I_D = 0, V_{GS} < V_{THN}$$

*Triode (linear) region*

$$I_D = \mu_n C_{ox}\frac{W}{L}\left((V_{GS} - V_{THN})V_{DS} - \frac{V^2_{DS}}{2}\right)$$

$$V_{GS} > V_{THN}, V_{DS} < V_{GS} - V_{THN}$$

*Saturation region*

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{THN})^2$$

$$V_{GS} > V_{THN}, V_{DS} \ge V_{GS} - V_{THN}$$

*Small-signal Parameters*

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{THN}) = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$

$$= \frac{2I_D}{V_{GS} - V_{THN}}$$

$$r_0 = \frac{1}{\lambda I_D}$$

**PMOS Equations**

Assuming all positive convention, make the substitutions in the above equations: $\mu_n \rightarrow \mu_p$, $V_{GS} \rightarrow V_{SG}$, $V_{DS} \rightarrow V_{SD}$, and $V_{THN} \rightarrow |V_{THP}|$

**NPN BJT Equations**

$$I_C \approx I_S e^{\frac{V_{BE}}{V_T}}\left(1 + \frac{V_{CE}}{V_A}\right), V_{BE} > 0$$

$$I_C = \beta I_B \quad I_E = (\beta + 1) I_B \quad I_C = \alpha I_E \quad \alpha = \frac{\beta}{\beta + 1}$$

*Forward Active Region:* $V_{BE} > 0, V_{CE} > V_{BE}$

*Saturation Region:* $V_{BE} > 0, V_{CE} < V_{BE}$

*Small-signal Parameters*

$$g_m = \frac{I_c}{v_T} \quad r_o = \frac{V_A}{I_C} \quad r_\pi = \frac{\beta}{g_m}$$

**For PNP BJT,** use above equations: $V_{BE} \rightarrow V_{EB}$ and $V_{CE} \rightarrow V_{EC}$

**Opamp Equations**

$$v_{out} = A(v_p - v_m)$$

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_1}}$$

*Negative feedback:*

$$A_{CL} \approx \frac{1}{\beta}\left(1 - \frac{1}{A_0\beta}\right)$$

$$\omega_{p,CL} \approx A_0\beta\omega_1 = \beta\omega_{un}$$

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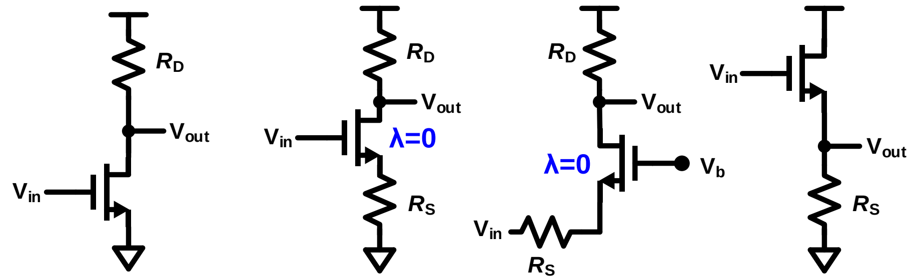
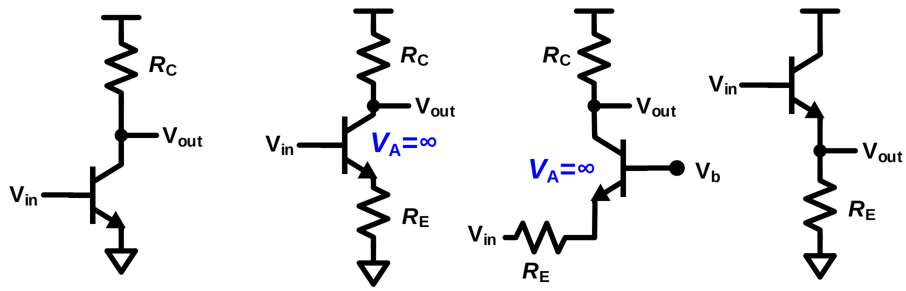
## Voltage Gain Equations

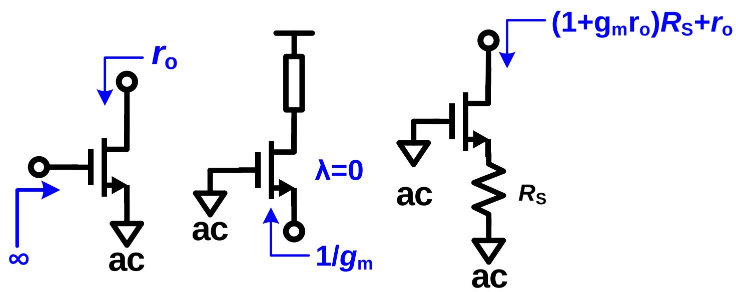


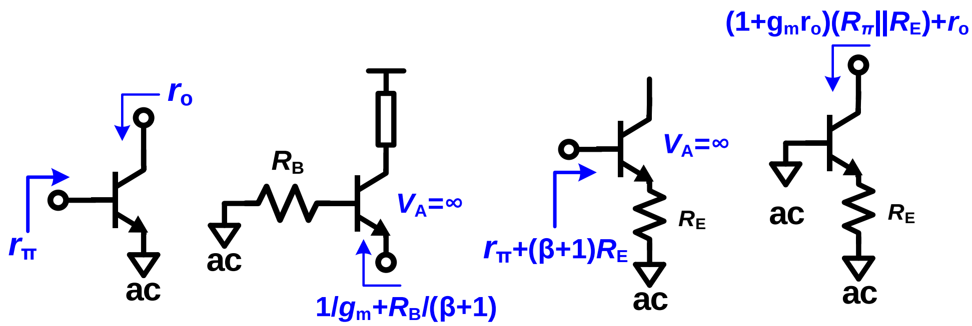

$A_v = -g_m(R_D \| r_o)$ $\quad A_v = \dfrac{-R_D}{1/g_m + R_S}$ $\quad A_v = \dfrac{+R_D}{1/g_m + R_S}$ $\quad A_v = \dfrac{R_S \| r_o}{1/g_m + R_S \| r_o}$




$A_v = -g_m(R_C \| r_o)$ $\quad A_v = \dfrac{-R_C}{1/g_m + R_E}$ $\quad A_v = \dfrac{+R_C}{1/g_m + R_E}$ $\quad A_v = \dfrac{R_E \| r_o}{1/g_m + R_E \| r_o}$

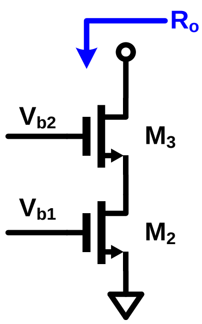
## Input and Output Impedances



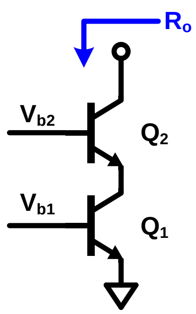



**1. (10 points)** Assume that the transconductances of all the transistors in this problem is equal to $\mathbf{g_m}$ and the output resistance is $\mathbf{r_o}$. Also, $V_{b1}$ and $V_{b2}$ are DC bias voltages. **Clearly show your work.**

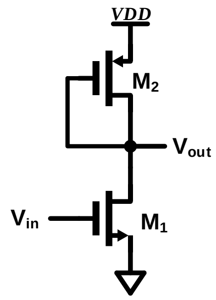
(a) (5 points) Assume that $M_1$ and $M_2$ are in saturation. Using small-signal analysis, find the output resistance ($R_o$) in the circuit shown below.

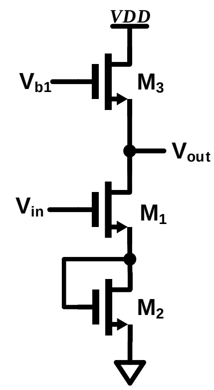


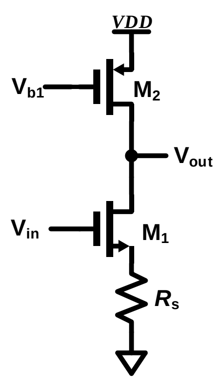

(b) (5 points) Assume that $Q_1$ and $Q_2$ are in active region. Using small-signal analysis, find the output resistance ($R_o$) in the circuit shown below.

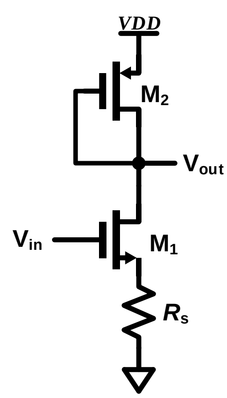


**2**. **(10 points)** Find small-signal voltage gain of the amplifier stages shown below in terms of transistor small-signal parameters $g_{m1}$, $g_{m2}$, $r_{o1}$, $r_{o2}$, $R_S$, $R_D$, etc. (Assume that all transistors are in saturation). $V_{b1}$, $V_{b2}$, etc., are DC bias voltages.

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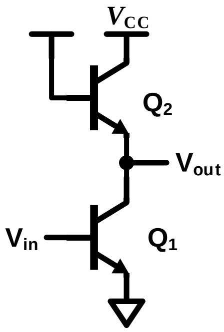
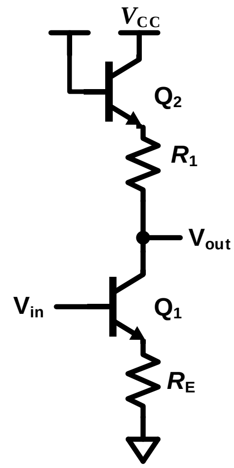
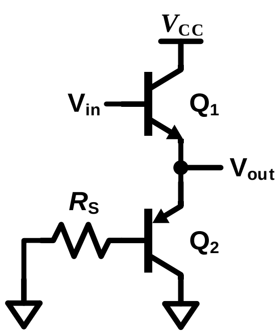
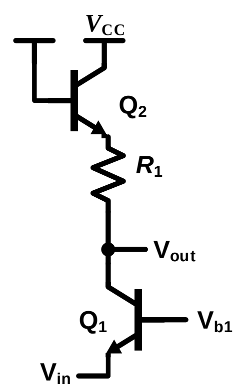
**3**. **(10 points)** Find small-signal voltage gain of the amplifier stages shown below in terms of transistor small-signal parameters $g_{m1}$, $g_{m2}$, $r_{o1}$, $r_{o2}$, $r_{\pi 1}$, $r_{\pi 2}$, $R_E$, etc. (Assume that all BJTs are in forward active region). $V_{b1}$, $V_{b2}$, etc., are DC bias voltages.



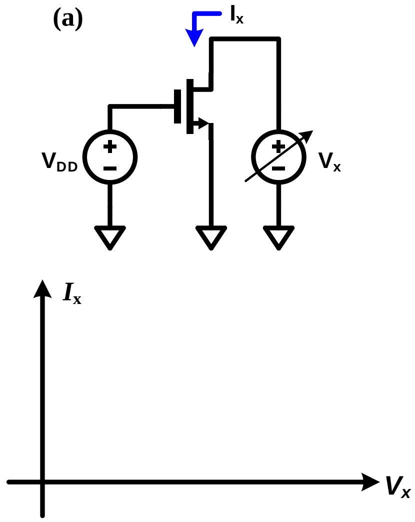



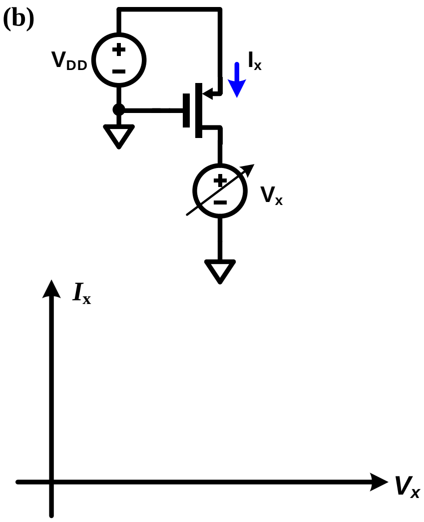



**4. (20 points)** For the circuits seen below, plot the quantity on the y-axis as the voltage $V_x$ is swept from 0 to $V_{DD}$=1.8V in parts (a,b & e) and 0 to $V_{CC}$=2.5V in parts (c&d). ***Label*** the plots and show your work for partial credit.

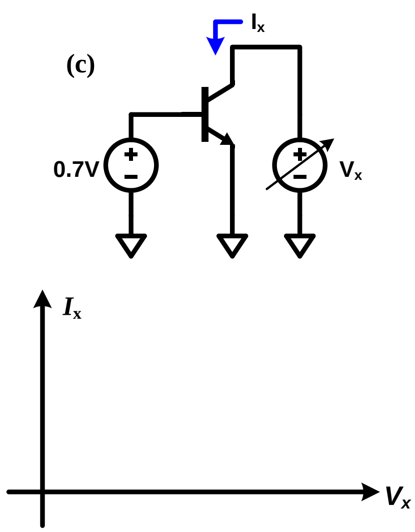
(a)



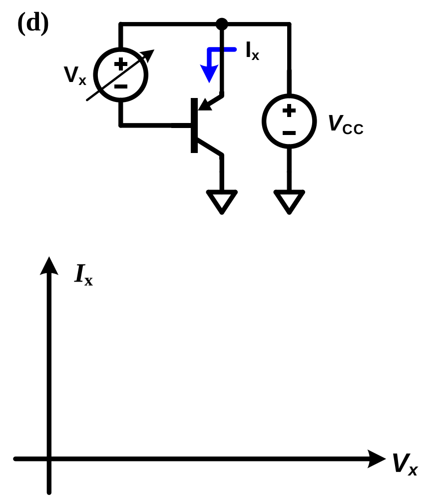

(b)



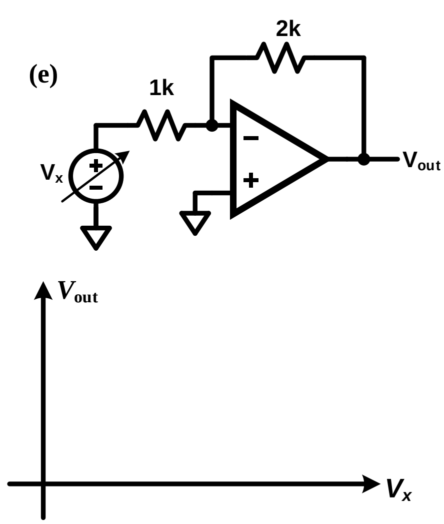

(c)



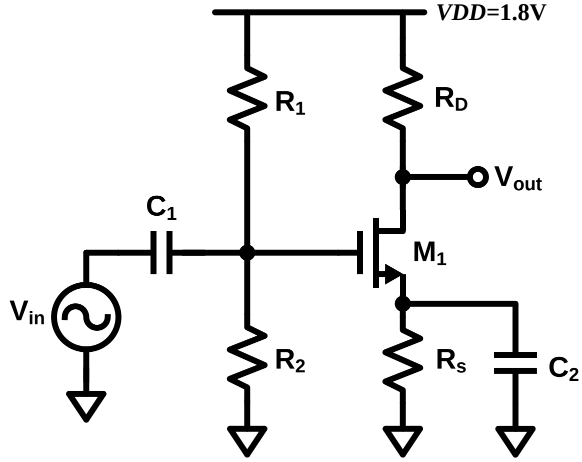

(d)




(e)



**5. (15 points)** Design the amplifier shown below for a voltage gain of **5**, an input impedance of **50kΩ**, and a total power budget of **5mW**. Assume that $\mathbf{V_{GS}=650mV}$ and the voltage drop of **400mV** across $R_s$. Assume that $C_1$ and $C_2$ are large, and $\lambda=0$.




(a) (2 points) Given the power budget for the transistor $M_1$, estimate the value of the bias current ($\mathbf{I_D}$).

(b) (3 points) Using part (a), Find the value of $\mathbf{R_s}$, $\mathbf{g_m}$ and $\mathbf{R_D}$.

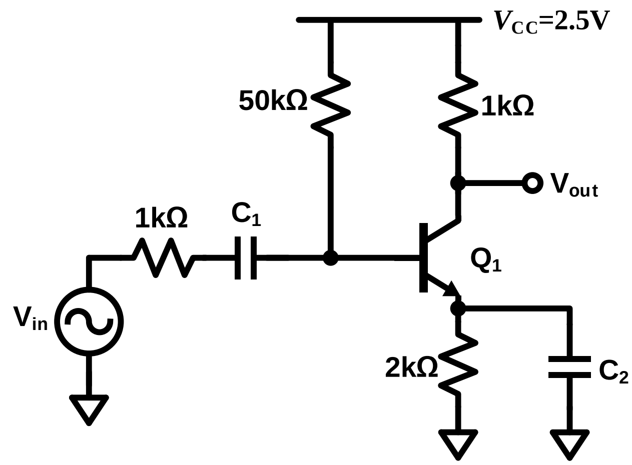
(c) (3 points) For the current, $I_D$, estimate the **W/L** ratio of the transistor.

(d) (2 points) Find the voltage at the gate of $M_1$, (**$V_G$**).

(e) (4 points) Given the input resistance and $V_G$ constraints, estimate the value of resistors **$R_1$** and **$R_2$**.

(f) (1 point) Verify whether $M_1$ is biased in saturation. If not, how will you fix this design?

**6. (15 points)** Consider the amplifier circuit shown below. Assume $C_1$ and $C_2$ are very large. *Use BJT data from the first page.*

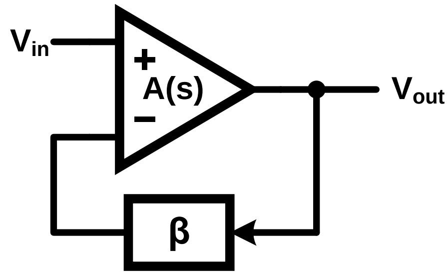



(a) (5 points) **Draw** the DC picture (i.e., the equivalent circuit considering only the DC quantities) for the amplifier and find **ALL** the node voltages in the circuit. Verify whether $Q_1$ biased in forward active region?

(b) (5 points) **Draw** the AC picture (i.e., the equivalent circuit considering only small-signal quantities) and find the small-signal gain ($\boldsymbol{A_v}$) of the amplifier. *Use forward active equations for $Q_1$.*

(c) (5 points) Find the small-signal input ($\boldsymbol{R_{in}}$) and output ($\boldsymbol{R_{out}}$) impedances of the amplifier.

**7. (20 points)** Consider the Opamp feedback circuit shown below. Here, β is the feedback factor, and the opamp transfer function is given by $A(s) = \dfrac{A_0}{\left(1 + \dfrac{s}{\omega_1}\right)}$.




(a) (7 points) Using the above Opamp, a **non-inverting** amplifier needs to be designed for a closed-loop gain, $\mathbf{A_{CL}=10}$, and a gain error of 1%. Determine the required open-loop gain ($\mathbf{A_0}$) of the opamp.

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(b) (6 points) Draw the schematic of the **non-inverting** amplifier in part (a) showing the required resistor values.

(c) (7 points) If the **non-inverting** amplifier in part (a) is to be designed for a closed-loop bandwidth of $\omega_{p,CL} = 2\pi \cdot 1MHz$. Determine the required unity-gain frequency ($\omega_{un}$) of the opamp.