Name: _____

EXAM #3

*Closed book, closed notes. Calculators may be used for numeric computations only. All work is to be your own - **show your work** for maximum partial credit.*

Data:

Use the following data in all the problems in the Exam:

V_{DD}	1.8V
$\mu_n C_{ox}$	200 μA/V^2
$\mu_p C_{ox}$	100 μA/V^2
V_{THN}	0.4V
$\lvert V_{THP}\rvert$	0.5V

NMOS Equations

Cutoff region

$I_D = 0, V_{GS} < V_{THN}$

Triode (linear) region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{THN}) V_{DS} - \frac{V^2_{DS}}{2} \right), V_{GS} > V_{THN}, V_{DS} < V_{GS} - V_{THN}$$

Saturation region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})^2, V_{GS} > V_{THN}, V_{DS} \geq V_{GS} - V_{THN}$$

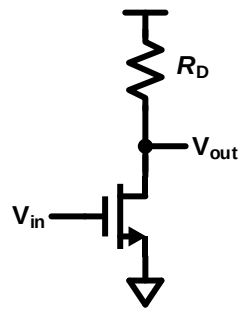
Small-signal Parameters

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN}) = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = \frac{2 I_D}{V_{GS} - V_{THN}}$$

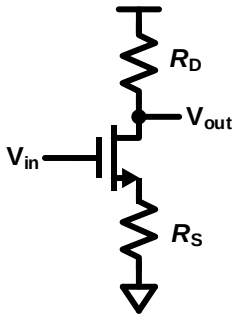
$$r_0 = \frac{1}{\lambda I_D}$$

PMOS Equations

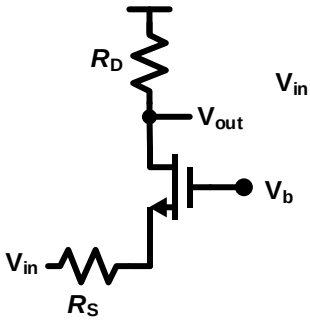
Assuming all positive convention, make the substitutions in the above equations: $\mu_n \rightarrow \mu_p$, $V_{GS} \rightarrow V_{SG}$, $V_{DS} \rightarrow V_{SD}$, and $V_{THN} \rightarrow |V_{THP}|$



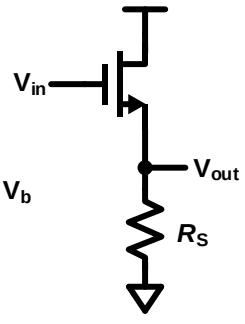
$A_v = -g_m(R_D \| r_o)$



$A_v = \dfrac{-R_D}{1/g_m + R_S}$



$A_v = \dfrac{+R_D}{1/g_m + R_S}$



$A_v = \dfrac{R_S \| r_o}{1/g_m + R_S \| r_o}$

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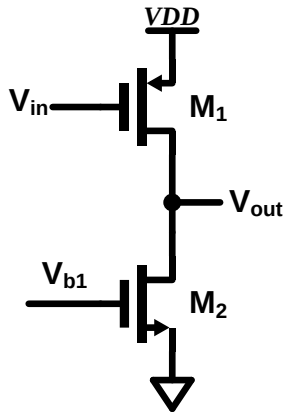
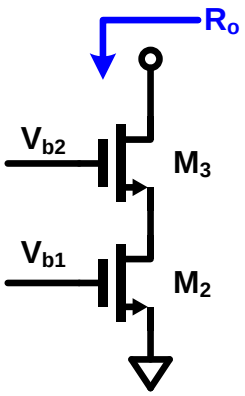
1. (25 points) **CMOS Amplifier Design**: Assume that the transconductances of all the transistors in this problem is equal to $\mathbf{g_m}$ and the output resistance is $\mathbf{r_o}$. Also, V_{b1} and V_{b2} are DC bias voltages. Clearly show your work.

(a) (5 points) Find the small-signal gain of the amplifier (in terms of g_m and r_o) shown below.



(b) (10 points) Assume that M_1 and M_2 are in saturation. Using small-signal analysis, find the output resistance (R_o) in the circuit shown below.



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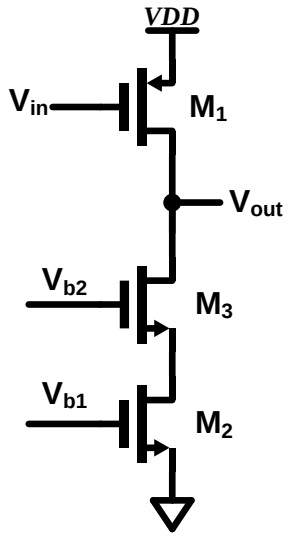
(c) (10 points) Using the result from part (b), find the small-signal gain of the amplifier shown below. Compare the answer with the result in part (a).



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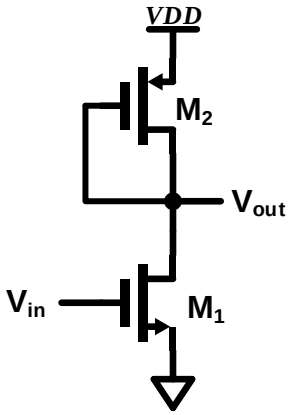
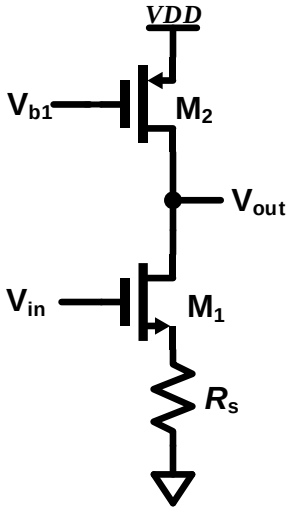
2. (25 points) Find small-signal voltage gain of the amplifier stages shown below in terms of transistor small-signal parameters g_{m1}, g_{m2}, r_{o1}, r_{o2}, Rs, etc. (Assume that all transistors are in saturation and $\lambda \neq 0$). V_{b1}, V_{b2}, etc., are DC bias voltages. Show your work.

(a)



(b)



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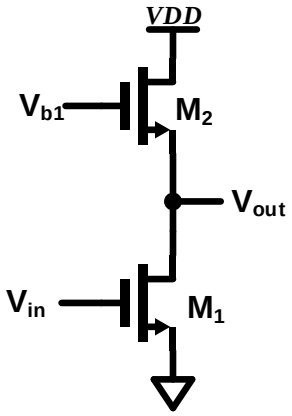
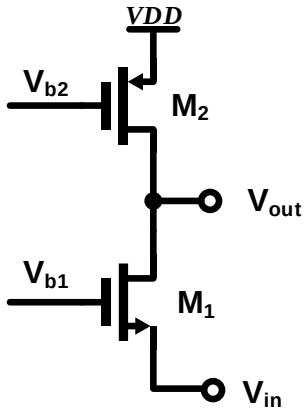
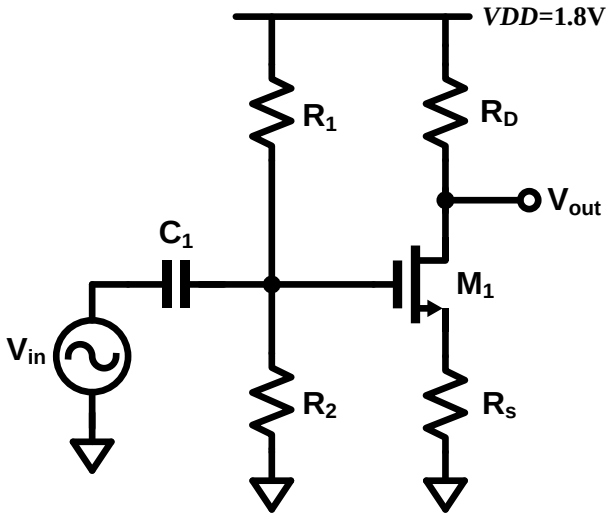
(c)



(d)



3. (25 points) Design a generated CS amplifier design following the given steps. The amplifier must provide a voltage gain of 4 with a power budget of 2mW while the drop across R_s is equal to 200 mV. The overdrive ($V_{ov}=V_{GS}-V_{THN}$) of the transistor M_1 should be 300mV and the total power consumed in the biasing resistances ($R_1 + R_2$) should be only 5% of the total power. Assume that C_1 is very large. *Use MOSFET data from the first page.*



(a) (4 points) Given the power budget for the transistor M_1, estimate the value of the bias current ($\mathbf{I_D}$).

(b) (4 points) Using part (a), find the value of $\mathbf{R_s}$.

(c) (4 points) For the current, I_D, estimate the **W/L** ratio of the transistor.

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(d) (5 points) Estimate the value of $\mathbf{R_D}$ for the required small-signal gain, A_v=4.

(e) (4 points) Find the voltage at the gate of M_1, ($\mathbf{V_G}$)

(f) (4 points) Using the 5% power budget constraint, and the gate voltage (V_G) estimate the value of resistors $\mathbf{R_1}$ and $\mathbf{R_2}$.

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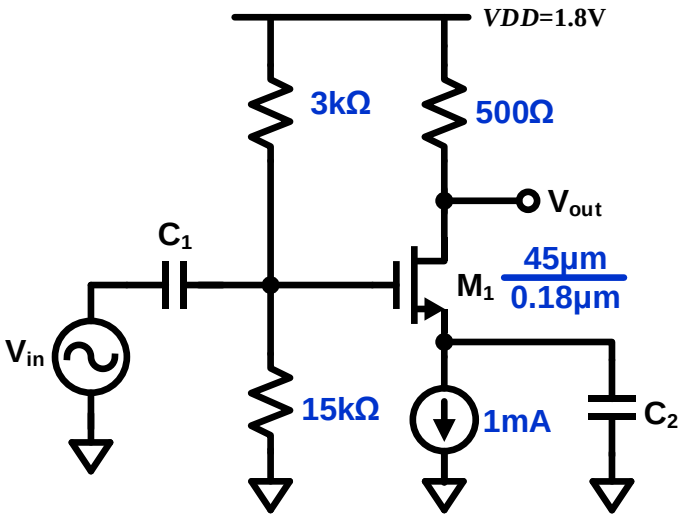
5. (25 points) Consider the amplifier circuit shown below. Assume C_1 and C_2 are very large. *Use MOSFET data from the first page.*



(a) (10 points) Draw the DC picture (i.e., the equivalent circuit considering only the DC quantities) for the amplifier and find ALL the node voltages in the circuit. Is M_1 biased in saturation?

(b) (10 points) Draw the AC picture (i.e., the equivalent circuit considering only small-signal quantities) and find the small-signal gain (A_v) and input impedance (R_{in}) of the amplifier.