1. **(90 points)** For the following loop:

   Loop:
   
   - L.D F2, 100(R1)
   - MUL.D F4, F2, F0
   - S.D F4, 100(R1)
   - ADD.D F0, F0, #10
   - SUB R1, R1, #4
   - BNEZ R1, Loop

   Assume that MUL.D takes 7 cycles of execution, ADD.D takes 4 cycles and branches are resolved in ID stage.

   a. **(10 points)** How many cycles does it take to execute this loop if no optimization is done?

   b. **(20 points)** Now rearrange instructions to get rid of as many stalls as you can. How many cycles does it take to execute this loop now?

   c. **(30 points)** How many times would you have to unroll this loop to get rid of the remaining stalls? Do this and show the unrolled loop. How many cycles per iteration we have now?

   d. **(30 points)** Assume that you can issue two instructions per cycle using VLIW. One of those should be integer instruction (load, store, integer ALU or branch) and the other should be a FP instruction. Show when each instruction is issued. How many cycles per iteration do we have now? On the average, how full is VLIW?