Microwave Properties of Silicon Junction Tunnel Diodes Grown by Molecular Beam Epitaxy

M. W. Dashiell, *Member, IEEE*, James Kolodzey, *Senior Member, IEEE*, P. Crozat, F. Aniel, and J.-M. Lourtioz, *Senior Member, IEEE*

***Abstract*—The bias dependence of the single-port microwave reflection gain of 15 μm-diameter Si Esaki tunnel diodes, grown by molecular beam epitaxy, was studied as a function of frequency. A simple equivalent circuit accurately modeled the data and yielded the forward-bias junction capacitance, which cannot be obtained by conventional low frequency capacitance–voltage techniques. The diodes were highly-doped step p-i-n junctions and exhibited a peak current density of 16 kA/cm^2. The microwave reflection gain and cutoff frequency were 12 dB and 1.6 GHz, respectively, with a speed index (slew rate) of 7.1 V/ns.**

***Index Terms*—Microwave measurements, molecular beam epitaxial growth, silicon, tunnel diodes.**

I. Introduction

TUNNEL diodes are attractive for high-performance circuits requiring fewer active devices to perform functions [1], [2]. Low-temperature molecular beam epitaxy (LTMBE) has produced highly doped silicon and silicon-germanium tunnel diodes of the p-n junction Esaki-type, and interband tunneling diodes with delta-doped layers [3]–[6]. Epitaxial diodes are anticipated to be compatible with integrated circuits, unlike the discrete metal-alloyed tunnel diodes that have been commercially available for decades [7]. The Si Esaki diode is especially promising for rapid integration, since it requires no SiGe epitaxy or thick SiGe relaxed buffer layers that are required for the more sophisticated Si/SiGe electron resonant tunneling diodes (RTDs) [8]. Relaxed SiGe buffers will not be as easily integrated into existent Si fabrication processes due to cost and reliability issues. This letter reports on the microwave reflection gain measurements of high-current-density silicon Esaki tunnel diodes grown on Si (001) by MBE and provides insight into their use in high-frequency applications.

The Esaki diodes were grown by LTMBE at 275 °C on 0.01 Ω-cm p$^+$ Si (001) substrates. The step *p-i-n* structure comprised a 15 nm B doped Si p-type buffer ($N_A = 1\times10^{19}$ cm^{-3}), a 15 nm B doped ($N_A = 4\times10^{20}$ cm^{-3}) Si p$^+$ layer, a 10-nm undoped spacer, and a 30 nm P doped ($N_D = 7\times10^{20}$ cm^{-3}) n^+ Si cap [3]. To reduce defects, the layers were annealed at 700 °C for 1 min after growth. Photolithography was used to fabricate 15 μm diameter mesa patterns. Large area concentric circular rings of evaporated Ti/Au metal formed planar microwave probable contacts on the Si surface for the ground signal, which were not annealed. Mesa isolation was achieved with reactive ion etching using the contact metal as an etch mask.

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M. W. Dashiell and J. Kolodzey are with the Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716 USA (e-mail: kolodzey@ee.udel.edu).

P. Crozat, F. Aniel, and J.-M. Lourtioz are with the Institute d'Electronique Fondamental, Universite Paris XI, 91405 Orsay, France.

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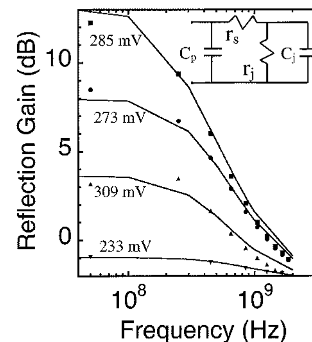

Fig. 1. Experimental reflected power gain Γ (solid points) of a typical epitaxial Si Esaki diode versus frequency and diode-junction voltage. The junction voltage was corrected for the series resistance. The modeled response (continuous lines) from the equivalent circuit (inset) used elements that gave the best fit to the data. The junction resistance (r_j) and depletion capacitance (C_j) were bias dependent, and the series resistance (r_s) and metal contact fringing capacitance (C_p) were bias independent.

Microwave measurements using a Hewlett Packard (Agilent) 8510C vector network analyzer were performed at a substrate temperature of 260 K. The microwave probes (PicoProbes) had the ground–signal–ground configuration with characteristic impedance $Z_o = 50\ \Omega$, calibrated by the short-open-load method. The microwave amplitude delivered to the diodes was less than 10 mV peak-to-peak. We confirmed that several representative diodes on the Si wafer were stable (i.e., no oscillations) in the negative differential resistance (NDR) region. The bias applied through the probes was incremented in 2 to 10 mV steps, and the single-port reflection coefficient (Γ) was measured from 50 MHz to 20 GHz with 101 evenly spaced frequency points. All junction voltages reported here were reduced to correct for the drop across the 6–7 Ω parasitic series resistance (r_s), determined by AC circuit modeling and dc measurements [3].

Fig. 1 shows the reflection gain (20log Γ) of the Si Esaki diode as a function of frequency for several different diode biases. The gain is very sensitive to bias, and the 12 dB value was representative of several diodes on the wafer. Biases of 273, 285 and 309 mV were in the NDR region, whereas 233 mV was below the NDR. The gain rolloff was −6 dB per frequency octave, with a cutoff frequency of 1.6 GHz, similar to the SiGe interband tunnel diodes with $J_p = 0.52$ kA/cm^2 presented in reference [6].

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A circuit model (inset to Fig. 1), with elements simply related to physical parameters, fit the microwave data well. It is notable that our circuit model is significantly simpler than the circuit model presented in reference [6]. The series resistance (r_s) and parallel fringing capacitance (C_p) were relatively bias independent, with values of 7 Ω and 50 fF, respectively. The junction resistance (r_j) and junction depletion capacitance (C_j) were bias dependent. These circuit elements were extracted using Touchstone software (EEsof-Agilent) to minimize the error (within ± 1 dB) between the modeled reflection coefficients and the data. Inductive reactance was negligible at these frequencies.

Fig. 2 summarizes the bias dependence of the gain versus frequency, and the corresponding negative differential conductance $(1/r_j)$. The highest gain occurred at the maximum modulus of $1/r_j$. At zero negative conductance, the power gain vanished. At the corrected junction voltage of 285 mV, the 12 dB gain corresponded to $r_j = -87\ \Omega$, which is itself well in agreement with that measured from the slope of the dc current–voltage characteristics $(-72\ \Omega)$. At this bias, the junction capacitance from microwave measurements was $C_j = 4$ pF. Due to the high conductance, we were not previously able to directly measure the tunnel diode's capacitance by conventional low-frequency capacitance–voltage (C–V) techniques.

From our extracted C_j, r_j, and r_s, the maximum resistive cutoff frequency, at which the diode no longer exhibits reflection gain, can be calculated [9]

$$f_{r0} = \frac{1}{2\pi |r_{j\,\min}| C_j} \sqrt{\frac{|r_{j\,\min}|}{r_s} - 1} = 1.52\ \text{GHz}. \tag{1}$$

This calculated frequency is in close agreement with the measured cutoff frequency.

The built-in potential V_{bi} and the reduced-doping concentration n^* were extracted from the intercept and slope of C_j^{-2} versus V_j shown in Fig. 3

$$\frac{1}{C_j^2} = \frac{2\left(V_{bi} - V_j - 2V_T\right)}{A^2 q \varepsilon_s n^*} \tag{2}$$

where V_T is the thermal voltage, A is junction area, q is the elementary charge, and ε_s is the Si permittivity. The n^* relates the tunneling current density to the width of the depletion tunneling barrier [3], [10], and was determined as $n^* = 6 \times 10^{19}$ cm^{-3} (steeper slope dotted line in Fig. 3) from microwave measurements in the NDR region. Our microwave C_j was consistent with calculations from the depletion width (4.6 nm at 0.285 V) inferred from the dc tunneling current—assuming the abrupt junction approximation with $V_{bi} = 1$ V [10] (see [3, Table I]). The junction capacitance determined from direct microwave measurement agrees well with the extractions from dc current characteristics in reference [3].

For biases above NDR, the Cj^{-2} yielded the voltage intercept of $V_{bi} - 2V_T = 1050$ mV, which is compared to calculations below. For the doping used here, the bandgap narrowing [11] of the built-in potentials is expected to be $\Delta E_G^{narrowing} = 125$ meV [10], [12]. The Fermi level extensions into the conduction and valence bands are $V_n = 27$ meV and $V_p = 69$ meV respectively, determined from n^* using Fermi–Dirac statistics [13]. The calculated $(V_{bi} - 2V_T)$ was $(E_G^{intrinsic} - \Delta E_G^{narrowing} + V_n + V_p - 2V_T)/q = 1046$ mV, in excellent agreement with experiment. At low bias in the NDR regime, the interpretation of the voltage axis intercept (380 mV) for the steeply sloped portion of the C_j^{-2} curve was uncertain.

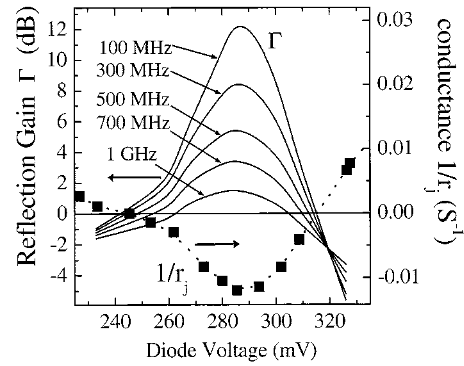

Fig. 2. Junction-voltage dependence of the reflected power gain (solid lines) of a typical Si Esaki diode for several frequencies and differential conductance (filled squares and dotted line). These parameters were from the equivalent circuit model giving the best fit to the data. The maximum gain occurred at the maximum absolute value of negative conductance $|-1/87\ \Omega|$.

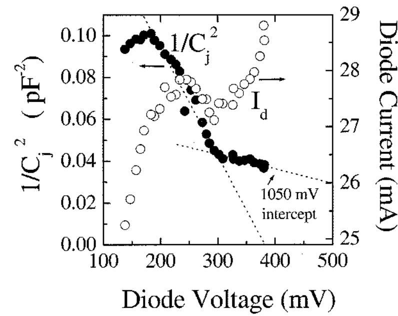

Fig. 3. Inverse-junction capacitance (C_j^{-2}) from microwave measurements versus the corrected junction voltage (V_j). Two slopes (referred to as steep and shallow) are observed, as explained in the text. From 200 to 300 mV, the steeper sloped dotted line for C_j^{-2} is drawn as a guide to the eye. The right axis shows the diode current at each bias during the microwave measurements.

The peak dc current of 28.7 mA in Fig. 3 corresponded to a current density of 16.2 kA-cm^{-2} and can be used to calculate the speed-index figure of merit. The speed index was $S = I_{peak}/C = 28.7$ mA/4 pF $= 7.1$ V/ns. We note that this speed index is a factor of seven greater than typical alloyed junction Si Esaki diodes listed in [7, Table I] and can be attributed to the higher current density of our diode. As discussed in [9], improvements in speed index are anticipated with miniaturization and design optimization.

II. Conclusion

The results in this letter demonstrated that MBE grown junction tunnel diodes are suitable for operation in the GHz frequency range. The microwave data fit a simple circuit model which yielded an accurate measurement of the junction capacitance, which cannot be obtained directly by conventional low frequency techniques.

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