

Room temperature operation of epitaxially grown Si/Si_{0.5}Ge_{0.5}/Si resonant interband tunneling diodes

Sean L. Rommel, Thomas E. Dillon, M. W. Dashiell, H. Feng, J. Kolodzey, and Paul R. Berger^{a)}
*Department of Electrical and Computer Engineering, University of Delaware, Newark,
Delaware 19716-3130*

Phillip E. Thompson and Karl D. Hobart
Naval Research Laboratory, Washington, D.C. 20375-5347

Roger Lake, Alan C. Seabaugh, Gerhard Klimeck,^{b)} and Daniel K. Blanks
Applied Research Laboratory, Raytheon Systems Company, Dallas, Texas 75243

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Resonant interband tunneling diodes on silicon substrates are demonstrated using a Si/Si_{0.5}Ge_{0.5}/Si heterostructure grown by low temperature molecular beam epitaxy which utilized both a central intrinsic spacer and δ -doped injectors. A low substrate temperature of 370 °C was used during growth to ensure a high level of dopant incorporation. A B δ -doping spike lowered the barrier for holes to populate the quantum well at the valence band discontinuity, and an Sb δ -doping reduces the doping requirement of the n -type bulk Si by producing a deep n^+ well. Samples studied from the as-grown wafers showed no evidence of negative differential resistance (NDR). The effect of postgrowth rapid thermal annealing temperature was studied on tunnel diode properties. Samples which underwent heat treatment at 700 and 800 °C for 1 min, in contrast, exhibited NDR behavior. The peak-to-valley current ratio (PVCR) and peak current density of the tunnel diodes were found to depend strongly on δ -doping placement and on the annealing conditions. PVCRs ranging up to

TABLE I. Summary of the room temperature I - V characteristics of Si/Si_{0.5}Ge_{0.5}/Si RITDs illustrating the peak voltage, peak current density, and PVCR for TD1 and TD2, and from mesa diodes of varying diameters. Results from the best devices are presented.

Sample number	Diode Diameter (μm)	Peak Voltage (V)	Peak current Density (A/cm^2)	PVCR
		700/800 °C	700/800 °C	700/800 °C
TD1	18	0.35/0.12	2150/220	1.21/1.04
	50	0.55/0.25	1720/180	1.18/1.04
	75	0.68/0.36	1490/470	1.11/1.35
TD2	18	0.34/0.16	3230/520	1.54/1.18
	50	0.87/0.38	2870/430	1.52/1.26
	75	1.21/0.52	2690/470	1.48/1.30

Stop growths are commonly employed to smoothen the growth front profile and reduce heterojunction roughness.^{12,13} During a stop growth, the growth rate drops considerably, but the impurity accumulation rate rises dramatically, which has been shown to quench quantum well photoluminescence.¹³ Also, dopant outdiffusion from the δ -doped spike is expected to be preferentially oriented towards the undoped central Si_{0.5}Ge_{0.5} spacer, rather than the highly doped outer Si injector layers, due to the concentration gradient. Furthermore, Sb diffusion^{14,15} has been shown to be enhanced with increased Ge content whereas B diffusion¹⁶ has been shown to be suppressed with the addition of Ge. Thus, the placement of the δ -doped layers offset from the Si_{0.5}Ge_{0.5} spacer using undoped Si in TD2 was expected to minimize these effects and to provide a higher quality tunneling barrier with reduced defects and higher PVCR. The data presented in this study supports this supposition (see Table I).

It is well known that dopants such as Sb can segregate during MBE growth, yielding undesirably broadened δ -doping profiles. Hobart *et al.* found that dopant segregation could be suppressed by lowering the growth temperature.¹⁷ Provided the layers are sufficiently thin, crystalline growth has been shown to occur even for extremely low temperatures (150 nm at 325 °C is a typical thickness).¹⁸ A short postgrowth anneal has been shown to be sufficient to activate the dopants and also to anneal out point defects.¹⁹ Therefore, in order to maximize the degeneracy of the δ -doping and bulk doping levels of the diodes in this study, a low substrate temperature of 370 °C was chosen with the understanding that an increase in point defect density might accompany the elevated doping levels.

Epitaxial growth was achieved with a specially designed MBE growth system²⁰ using elemental Si and Ge in e -beam sources, elemental Sb in a standard Knudsen cell and elemental B in a high temperature Knudsen cell. The structures were grown on 75 mm B-doped ($\rho=0.015-0.04 \Omega \text{ cm}$) Si(100) wafers. Prior to growth, the substrates were prepared using a cleaning technique previously described.²¹ Base pressure of the MBE growth system was 5×10^{-9} Pa and typical pressure during growth was 6×10^{-7} Pa. The growths were initiated with a 1 nm undoped Si buffer layer grown at 700 °C. The substrate temperature was then lowered to 540 °C for the growth of a 70 nm B-doped p^+ -Si ($2 \times 10^{19}/\text{cm}^3$) layer. The substrate temperature was further reduced to 370 °C for the remainder of the sample growth.

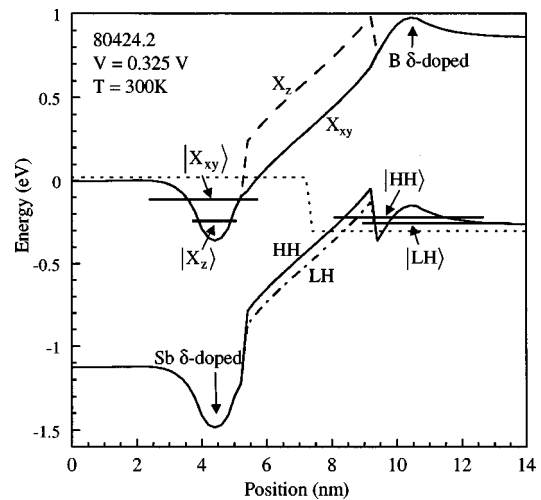


FIG. 2. Calculated band diagram of the RITD using the TD2 structure illustrated in Fig. 1(b).

This included a B δ -doped layer ($7 \times 10^{13}/\text{cm}^2$), an undoped tunneling barrier (see Fig. 1), an Sb δ -doped layer ($3 \times 10^{14}/\text{cm}^2$), and a 100 nm Sb-doped n^+ -Si ($4 \times 10^{19}/\text{cm}^3$) contact layer. All regions of the sample were grown at a rate of 0.1 nm/s with the exception of the Si_{0.5}Ge_{0.5} spacer, which was grown at 0.08 nm/s.

Prior to device fabrication, portions of the wafers were annealed using a forming gas ambient in an AG Associates Heatpulse 610 RTA furnace at 600, 700, or 800 °C. All anneal times were held constant at 1 min. A series of Al dots with 18, 50, and 75 μm diameters were patterned on the surface of the wafers via a standard contact lithography/liftoff process. A buffered oxide etch was used prior to metallization. Using the Al dots as a self-aligned mask, a series of mesas were etched in a CF₄/O₂ plasma which resulted in some undercutting of the metal mask. Finally, an Al backside contact was thermally evaporated on all of the samples.

Figure 2 shows a calculated band diagram of tunnel diode TD2 described in Fig. 1(b). The δ -doped regions are assumed broadened over 1 nm with a dopant activation of 50%. The effective-mass Schrödinger equation and corresponding quantum charge is solved for each band and iterated to convergence with Poisson's equation. The strain in the Si_{0.5}Ge_{0.5} splits the light hole and heavy hole bands by 80 meV, and it splits the X_z and X_{xy} valleys of the conduction band by 310 meV where z is the direction of crystal growth. The δ -doping provides two charge planes which determine the built-in voltage across the tunnel region. The Sb δ -doping reduces the doping requirement of the n -type bulk Si by producing a deep n^+ well. The heterojunction provides a corresponding p^+ well in the valence band, and the B δ doping reduces the barrier to holes entering the well. The light- and heavy-hole states align with the X_z electron state at 0.30 and 0.34 V, respectively. The peak current is assumed to occur in this range of voltages.

Current-voltage (I - V) characteristics were measured with an HP 4142 Semiconductor Parameter Analyzer and a Tektronix curve tracer. All measurements were compared on both systems for consistency. The as-grown RITDs showed no signs of NDR, and exhibited I - V characteristics of leaky backward diodes.

In contrast, samples which were annealed at 700 and

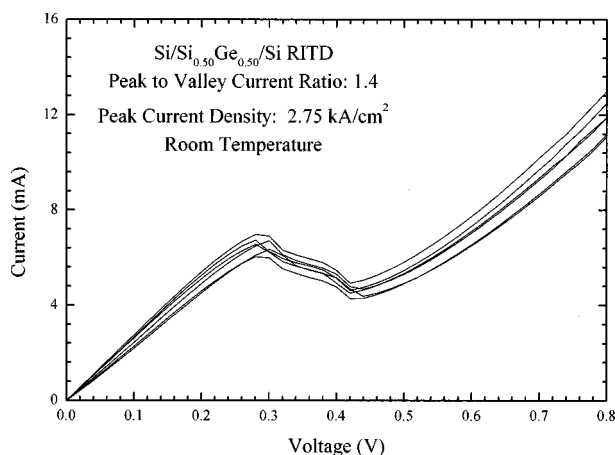


FIG. 3. I - V characteristics of six representative RITDs with the TD2 structure annealed at 700 °C having 18 μm diameters which exhibit room temperature NDR (PVCR \sim 1.4 at a peak current density of 2.75 kA/cm 2).

800 °C exhibited room temperature NDR behavior (Table I and Fig. 3). TD2 was also annealed at 600 °C and only showed a plateau in its I - V characteristics near the peak voltage where NDR was observed for the samples annealed at 700 and 800 °C. Furthermore, from Table I, lower PVCR and peak current density (by an order of magnitude) is observed for annealing temperatures as high as 800 vs 700 °C. A key observation is that the peak current density can be engineered during postgrowth processing with a short high temperature anneal. Optimal annealing temperatures appear to be between 600 and 800 °C, perhaps close to the 700 °C employed here.

An interesting trend was found among the samples tracking the placement of the δ -doping plane. TD1, the structure with the δ doping placed at the heterointerface, was found to have PVCRs which ranged up to 1.21 with a peak current density of 2.1 kA/cm 2 and 1.35 with a peak current density of 470 A/cm 2 when annealed at 700 and 800 °C, respectively. TD2, where the δ doping was offset 1 nm from the SiGe/Si heterointerface, exhibited PVCRs up to 1.54 with a peak current density of 3.2 kA/cm 2 and 1.30 with a peak current density of 470 A/cm 2 when annealed at 700 and 800 °C, respectively. With the exception of the 75- μm -diam diode from TD1 annealed at 800 °C, the performance of the remainder of the devices appeared to improve with the δ -doping plane offset 1 nm away from the Si/SiGe heterointerface. The aforementioned discrepancy in the data is attributed to a known radial nonuniformity in the B dopant distribution of the samples.

The peak voltages measured for all the samples shifted to higher voltage with increasing diode area due to series resistance. By plotting the peak voltage versus the peak current as a function of diode diameter, the slope of the curve yields an intrinsic series resistance of 5 Ω in the measurement setup. The extrapolated intrinsic peak voltage for TD2 annealed at 700 °C was found to be 0.33 V, from the y intercept, which agrees favorably with the predicted value obtained from theoretical modeling, Fig. 2.

It should be noted that the I - V characteristics for all the diodes measured in this study were repeatable and stable. Some RITDs were tested continuously for up to 1 h and without degradation in PVCR. Also, the yield of RITDs ex-

hibiting NDR behavior is estimated over 95% from the samples annealed at 700 to 800 °C. Figure 3 shows an overlay of the I - V characteristics obtained from six representative RITDs from TD2 (annealed at 700 °C) to illustrate NDR reproducibility.

In conclusion, NDR behavior at room temperature was observed in epitaxially grown Si/SiGe/Si heterostructure RITDs. The structures utilized an intrinsic Si $_{0.5}$ Ge $_{0.5}$ tunneling barrier and δ -doped Si injectors. The placement of the δ -doping plane offset into the Si injectors may have reduced the effect of impurity diffusion of dopants into the central device region. Low temperature epitaxial growth at 370 °C allowed for a high incorporation of dopant species. Subsequent postgrowth anneals were found to activate the dopants and reduce point defect density, and an optimal anneal temperature appears to exist. NDR behavior was observed to be stable and repeatable. This study has demonstrated that SiGe RITD peak current density and PVCR can also be tailored by appropriate postgrowth processing.

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