Reduced lattice temperature high-speed operation of pseudomorphic InGaAs/GaAs field-effect transistors

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This letter presents a detailed study of the temperature dependence of submicron pseudomorphic InGaAs on GaAs substrate modulation doped field-effect transistors (MODFETs), doped-channel metal insulator field effect transistors (MISFETs), and metal semiconductor field-effect transistors (MESFETs). We determine similar variation in the measured extrinsic current gain cutoff frequency, \( F_T \), and similar dependencies of the effective electron velocity, \( \nu_{\text{eff}} \), with reduced lattice temperature for the different field-effect transistors. The \( \nu_{\text{eff}} - T^{-b} \) where \( 0.15 < b < 0.20 \) over the temperature range of 300 to 110 K. These results provide direct experimental evidence that the saturated velocity of electrons is the most important parameter for high-speed operation and with proper design these different pseudomorphic InGaAs/GaAs field-effect transistors provide similar potential for high-speed operation.

The advent of a reproducible cryogenic microwave measurement system \(^1\) has allowed for detailed studies of the reduced lattice temperature operation of pseudomorphic InGaAs/GaAs field-effect transistors (FETs). Recent results include cryogenic high-speed measurements of doped-channel metal insulator field-effect transistors (MISFETs), \(^2\) modulation doped field-effect transistors (MODFETs), \(^3\) and metal semiconductor field-effect transistors (MESFETs). \(^4,5\) The MODFET is attractive for the enhanced electron mobility achieved by reduced ionized impurity scattering as the result of spatially separating the electrons from the ionized donors. The doped-channel MISFET is distinguished by a narrow-gap active channel and undoped wide-gap insulator, which is opposite to the MODFET doping scheme. The advantages of this device design includes higher current drivability and higher breakdown voltage. The MISFET is attractive since donors can be directly ion implanted into the substrate increasing the potential for high manufacturing throughput and reliability. A surprising trend, however, has been the similar high-speed performance of the different FETs for gate lengths from 1.0 to 0.1 \( \mu m \). \(^6\) The recent results in the literature raise the question of how significant are the contributions of high-electron mobility and two-dimensional electron transport in the high-speed operation of InGaAs/GaAs FET performance.

In this letter we report a detailed study of the temperature dependence of pseudomorphic InGaAs on GaAs substrate MODFETs, doped-channel MISFETs, and MESFETs. We determined similar increases in the measured extrinsic \( F_T \) and similar dependences of the effective electron velocity, \( \nu_{\text{eff}} \), with reduced lattice temperature for the different FETs.

The MODFET structure used in this study was grown by solid-source molecular beam epitaxy (MBE) and consists of a 1 \( \mu m \) GaAs buffer, 170 A In\(_{0.25}\)Ga\(_{0.75}\)As strained channel, 50 \( \AA \) undoped Al\(_{0.25}\)Ga\(_{0.75}\)As undoped spacer, Al-doped Si plane with areal density \( 6 \times 10^{12} \) \( \text{cm}^{-2} \), 350 A undoped Al\(_{0.25}\)Ga\(_{0.75}\)As insulator, and a 200 \( \AA \) cap layer of n-GaAs Si doped to \( 2.7 \times 10^{18} \) cm\(^{-3} \). The MODFET was grown by metalorganic chemical vapor deposition and consists of an undoped 600 A In\(_{0.15}\)Ga\(_{0.85}\)As layer, and an undoped 1000-\( \AA \)-thick layer of In\(_{0.1}\)Ga\(_{0.9}\)As with the In composition graded from 0.18 to 0 at the surface for an improved Schottky barrier height. The active channel of the MESFET is formed by ion implanted Si + 29 ion species and subsequent capless annealing at 850 °C for 20 min. The peak carrier concentration in the channel is \( 2 \times 10^{18} \) \( \text{cm}^{-3} \). The doped-channel MISFET was grown by solid source MBE and consists of a 1 \( \mu m \) GaAs buffer, 150 A In\(_{0.35}\)Ga\(_{0.65}\)As strained channel Si doped to \( 5 \times 10^{16} \) cm\(^{-3} \), 250 A undoped Al\(_{0.35}\)Ga\(_{0.65}\)As insulator, and a 200 \( \AA \) cap layer of n-GaAs Si doped to \( 5 \times 10^{18} \) cm\(^{-3} \).

An electron-beam direct write process has been used to define “T-shaped” gates with device isolation achieved by wet chemical etching. The MESFETs in this study have gate dimensions of 0.25\( \times \) 200 \( \mu m \) and 0.5 \( \times \) 200 \( \mu m \) with a source-drain spacing of 2 \( \mu m \). The MODFETs have gate dimensions of 0.35 \( \times \) 100 \( \mu m \) and 0.47 \( \times \) 100 \( \mu m \) with a source-drain spacing of 1 \( \mu m \). The MISFETs have gate dimensions of 0.25 \( \times \) 100 \( \mu m \) with a source-drain spacing of 1 \( \mu m \).

S-parameter data was collected from 0.5 to 26.5 GHz using a Hewlett-Packard 8510 B network analyzer. Measurements have been made at a temperature of 300 K using a Cascade model 42 D high-frequency probe station and at 110 K using a custom-built cryogenic high-frequency probe station. \(^4\) Calibrations were performed “off-water” using an impedance standard substrate from Cascade Microtech. The measured s parameters are used to calculate the \( h \) parameters. In Fig. 1, we plot typical \( |h_{21}| \) versus...
frequency results for a $0.25 \times 200 \ \mu m$ InGaAs/GaAs MESFET at 300 and 112 K. We observe no evidence of resonance or inductive effects and the current gain follows a $-6 \ \text{dB/octave}$ roll-off which extrapolates to the unity short-circuit current gain cut-off frequency, $f_T$. The measured peak $f_T$ improves from 104 to 122 GHz when the lattice temperature is reduced from 300 to 112 K.

In Fig. 2, we plot the typical percentage change from 300 to 110 K in the extrinsic $f_T$ for the three FET structures for gate lengths between 0.5 and 0.25 $\mu m$. When the effect of pad parasitics is removed the percentage increase in $f_T$ is less than 30% for all devices. The peak $f_T$ at 300 K is 104 GHz for the MESFET, 88 GHz for the MODFET, and 56 GHz for the doped channel MISFET.

A detailed analysis of the extrinsic $s$ parameters has been made to extract the intrinsic device parameters. It is important to extract the intrinsic device parameters to accurately measure the trends of important physical parameters for different device structures and different lattice temperatures. The hybrid-$\sigma$ equivalent circuit of Fig. 3 was used to fit the measured $s$ parameters. The circuit analysis technique originally proposed in Ref. 7 is used to help to uniquely identify the small-signal element values. The pad parasitics were determined by measuring a gateless device with the technique outlined in.

Once the small-signal element values have been determined and the values validated by fitting to the equivalent circuit of Fig. 3 we estimate an effective electron velocity, $v_{\text{eff}}$, from:

$$v_{\text{eff}} = L_g \frac{g_m}{C_{gs} + C_{dg}}.$$  \hfill (1)

The $v_{\text{eff}}$ is then plotted versus temperature in Fig. 4. Hall-effect measurements for the MODFETs used in this study show that the electron mobility increases by a factor of five when the lattice temperature is reduced from 300 to 77 K. The electron mobility decreases by 2% in the doped channel MISFET and decreases by 7% in the MESFET. Independent determination for 5% indium channel MODFETs have shown a saturated velocity increase of 20% when the lattice temperature is reduced from 300 to 100 K. These results are important for they provide direct experimental evidence that the low-field electron mobility is not the dominant factor in determining the high-speed performance of InGaAs/GaAs FETs. Similar conclusions about
FIG. 5. Plot of the ratio of $C_{gs}/C_{gd}$ vs $g_{m}/g_{out}$ for all InGaAs/GaAs FETs measured in this study. The data include results over the temperature range of 300–110 K. The measured data fit well to a slope, $\beta$, of $-0.27$ which agrees well with 300 K results reported in Ref. 11.

the relevance of electron mobility for high-speed performance have been drawn from recent results in the literature.4,10

To gain insight into the physical mechanisms controlling high-speed operation we have applied a feedback correlation analysis as originally proposed in Ref. 11:

$$C_{gs}/C_{gd} = 1 + \beta \frac{g_m}{g_{out}}$$

where $C_{gs}$ is the gate-source capacitance, $C_{gd}$ is the drain-gate capacitance, $g_m$ is the transconductance, $g_{out}$ is the output conductance, and $\beta$ is an empirical fitting parameter. We can determine the parameter $\beta$ by plotting $C_{gs}/C_{gd}$ versus $g_{m}/g_{out}$. Since $g_{out}$ increases as current spreads out of the conducting channel, and $g_m$ represents control of the channel current, the ratio $g_{m}/g_{out}$ is a measure of the confinement of rf current. A small value of $\beta$ results in a large $g_{m}/g_{out}$ ratio reflecting good current confinement in the drift region of the device (high-voltage gain and small output conductance).

In Fig. 5 we plot $C_{gs}/C_{gd}$ versus $g_{m}/g_{out}$ for the three different FETS for several different devices over a temperature range from 300 to 110 K. We find $\beta = 0.27$ for all the devices over the temperature range 300 to 100 K which agrees quite well with the value of $\beta \sim 0.3$ extracted in Ref. 11 for 300 K measurements. This analysis not only confirms the previous trends observed in the literature but also reveals that there is no enhanced carrier confinement under high fields at reduced lattice temperatures for these InGaAs/GaAs FETS.

In conclusion, based on detailed cryogenic microwave measurements of pseudomorphic InGaAs/GaAs MODFETs, doped channel MISFETs, and MESFETs we find a similar variation of $v_{sat}$ with temperature. Because of the high-electric fields associated with submicron FET operation the saturated velocity of electrons in the gate-drain portion of the transistor is the most important parameter for high-speed operation. We find no evidence of enhanced carrier confinement in either reduced lattice temperature operation or in the two-dimensional quantum well structures. These results provide direct experimental evidence that with proper device design these different pseudomorphic InGaAs/GaAs FET structures all provide good potential for high-speed operation.

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