Direct-current and radio-frequency properties of InAlAs/InGaAs pseudomorphic modulation doped field effect transistors with graded channels

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We report comprehensive high-frequency characteristics of pseudomorphic InAlAs/InGaAs/InP modulation doped field effect transistors having thick, dislocation-free channels with an In mole fraction compositionally graded to $x = 0.65$ at the heterointerface. Grading was achieved by reducing the Ga effusion cell temperature during epitaxial growth. High-frequency S-parameter measurements were performed on transistors having gate lengths of $L_g = 0.25$ μm and showed significant increases in both transconductance g_m and current gain cutoff frequency f_T with increasing graded channel layer thickness. The best devices with a 30 nm channel have $g_m = 720$ mS/mm and $f_T = 120$ GHz. We give data on growth conditions, layer structure, and device electrical properties.

I. INTRODUCTION

The performance of modulation doped field effect transistors (MODFETs) depends strongly on the transport properties of the conducting channel region. For several material systems, state-of-the-art values of extrinsic transconductance g_m and current gain cutoff frequency f_T for MODFETs are: $g_m = 410$ mS/mm and $f_T = 113$ GHz for AlGaAs/GaAs with gate length $L_g = 0.1$ μm[1]; $g_m = 700$ mS/mm and $f_T = 175$ GHz, for lattice-matched $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ with $L_g = 0.2$ μm;[2] and $f_r = 1160$ mS/mm and $f_T = 210$ GHz, for pseudomorphic $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As/InP$ having In mole fraction $x = 0.65$ and $L_g = 0.1$ μm.[3] For pseudomorphic layers on InP, values of x exceeding 0.53 result in misfit dislocations if the layer thickness exceeds a critical value t_{crit}. In this paper, we show that values of $x = 0.65$ at the heterointerface are compatible with relatively thick channel layers without dislocations if the composition of the channel layer is graded from the lattice-matched value at the substrate. The grading is achieved during molecular-beam epitaxy (MBE) by reducing the Ga cell temperature, which increases the In mole fraction continuously. We show that MODFETs made by this technique have excellent properties and no misfit dislocations. The thickness values are consistent with the Ball–Van der Merwe (BVM) criterion for compositionally graded layers.

II. STRUCTURE GROWTH AND PROPERTIES

The structure layers were grown by MBE in a Riber system on semi-insulating InP and are shown in Fig. 1. The growth rate was typically 1 μm/h, the substrate temperature was 575 °C, and the background pressure during growth was 4×10^{-7} Torr. The 500 nm InAlAs wide energy gap barrier layer reduces impurity diffusion from the substance. The 500 nm undoped InGaAs layer helps smooth the interface and serves as the conducting channel for the lattice-matched control structure. To achieve grading, InGaAs channel layer thicknesses of $d_{chan} = 0$, 20 and 30 nm were grown by reducing the Ga effusion cell temperature T_{Ga} from 948 °C for the lattice-matched composition $x = 0.53$ to 918 °C yielding $x = 0.65$ at the heterointerface. Immediately after growing the graded layer, T_{Ga} was raised again to prepare for the final cap layer. The upper $In_{0.52}Al_{0.48}As$ layers were grown

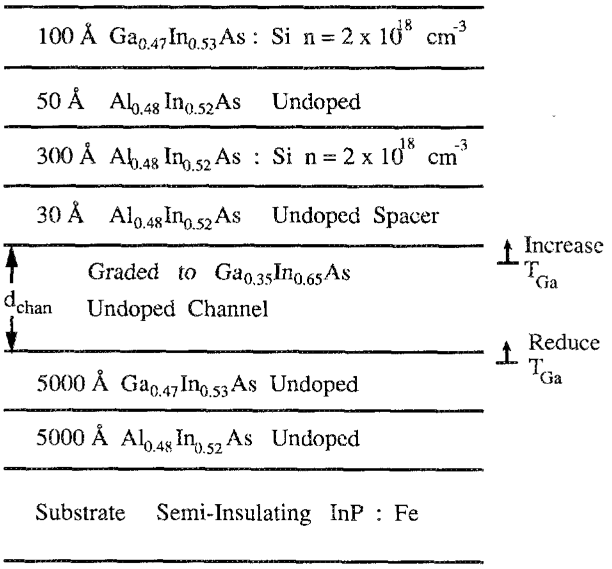

FIG. 1. Cross section of MODFET layer structure and dimensions. Graded InGaAs channel layer thicknesses are $d_{chan} = 0$, 20, and 30 nm.

at the lattice-matched composition and comprise: an undoped spacer, a Si-modulation doped region with electron concentration $n = 2\times 10^{18}$ cm^{-3}, and an undoped Schottky gate contact layer. Finally, a lattice-matched InGaAs cap doped with Si to $n = 2\times 10^{18}$ cm^{-3} is used for ohmic source and drain contacts.

To evaluate the materials, we used Hall measurements and dark field transmission electron microscope (TEM) imaging. Hall results at temperatures of 300 and 77 K are given in Table I for the three structures with differing d_{chan}. The electron mobility μ_n increases significantly with d_{chan}. We attribute the larger mobility of the $d_{\text{chan}} = 300$ nm structure to the larger values of x within 10 nm of the heterointerface which contains most of the electron wave function. There is no clear trend of electron sheet density versus d_{chan} and we attribute this to unintentional variation of the Si density in the layers and perhaps Hall contact asymmetries.

Dark field TEM image analysis for the three structures indicates that no misfit dislocations are present.[4] The contrast variation of the TEM images also indicates that the composition variation was gradual. To compare the channel layer thicknesses with theoretical expectations, we calculated the critical thickness t_{crit} based on two models of lattice strain. In Fig. 2, we plot (a) the Matthews–Blakeslee (MB) criterion t_{crit} for uniform layers versus In mole fraction,[5] and (b) the BVM criterion t_{crit} for graded composition layers versus grading slope parameter[6]:

$$S = \frac{\Delta x}{d_{\text{chan}}}, \tag{1}$$

where Δx is the difference between the mole fraction of the graded layer endpoints. For $d_{\text{chan}} = 30$ nm we have $S = 4.0$ per μm, yielding t_{crit} (BVM) = 45 nm. This graded channel value exceeds the d_{chan} which at 29 nm would be the limit for a uniform composition channel having $x = 0.65$. Figure 2 accounts for a double-kink mechanism appropriate for buried misfit layers and the critical thicknesses are therefore twice the single-kink values for surface layers that are sometimes quoted.

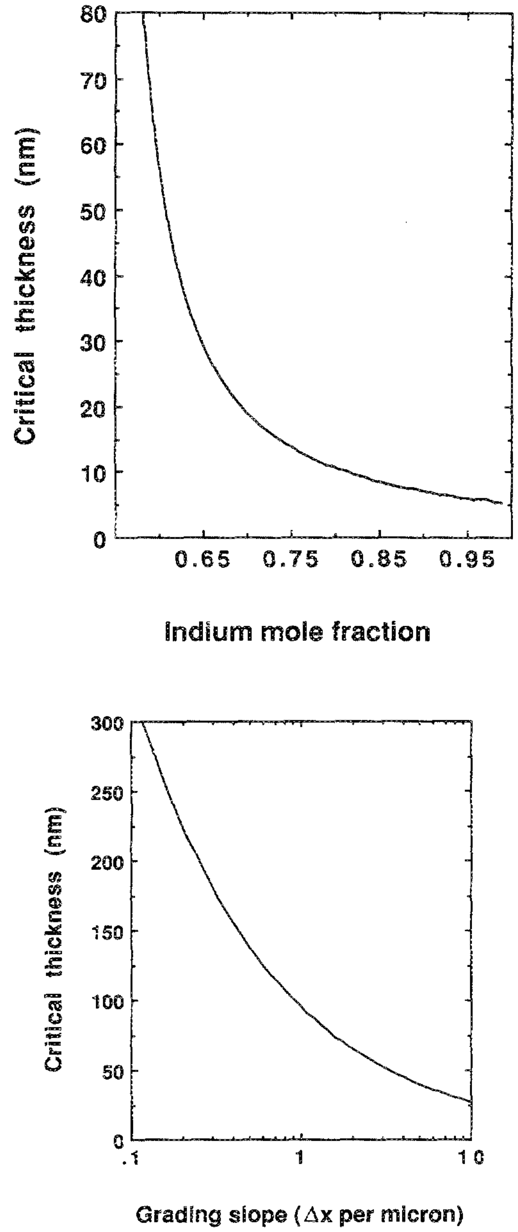

FIG. 2. Plots of (a) critical thickness from the MB criterion t_{crit} for uniform layers vs In mole fraction x and (b) critical thickness from the BVM criterion t_{crit} for graded composition layers vs grading slope parameters $S = \Delta x/d_{\text{chan}}$.

III. DEVICE FABRICATION AND PROPERTIES

We fabricated submicron MODFETs to investigate the effects of channel grading on device performance. For all devices, the gate length is $L_g = 0.25$ μm with a "T"-shaped cross section, the drain source separation is 1 μm, and the gate width is 100 μm. Photolithography was used for the device isolation mesas and for the source and drain ohmic contacts. A Cambridge EBMF-6.5 electron beam lithography system was used to write the submicron gate patterns. Source/drain metals are alloyed Au/Ge/Ni/Au, and the gate metal is Ti/Au. All metals were deposited by electron beam evaporation and patterned by a lift-off process. The contact patterns were designed to be compatible with coplanar transmission line probes from Cascade Microtech. Further processing details are given in Ref. 7.

Values of extrinsic transconductance $g_m = \partial I_D/\partial V_{GS}$ from dc current–voltage measurements for the three thicknesses are given in Table II along with other parameters to be described later, showing that g_m increases significantly with d_{chan}.

TABLE I. Hall measurement results giving electron mobility μ_n and electron sheet density n_s at 300 and 77 K for InAlAs/InGaAs modulation doped structure depicted in Fig. 1 vs d_{chan}.

d_{chan} (nm)	300 K μ_n (cm^2/V s)	77 K μ_n (cm^2/V s)	300 K n_s ($\times 10^{12}$ cm^{-2})	77 K n_s ($\times 10^{12}$ cm^{-2})
0	8 380	43 200	2.65	2.25
20	9 190	58 200	3.00	2.38
30	12 500	64 900	2.12	2.05

TABLE II. Measured values of: cutoff frequencies f_T, $f_{\max}$, and dc value of extrinsic g_m (dc); and values of: gate capacitances C_{gs} and C_{gd} and g_m (rf) extracted at a frequency of 5 GHz, vs channel thickness d_{chan} for MODFET having $L_G = 0.25$ μm.

d_{chan} (nm)	f_T (GHz)	$f_{\max}$ (GHz)	C_{gs} (fF)	C_{gd} (fF)	rf g_m (mS/mm)	dc g_m (mS/mm)
0	100	80	75.0	13.4	613	370
20	106	100	72.0	17.2	666	565
30	120	100	71.1	22.8	765	720

IV. HIGH FREQUENCY PERFORMANCE

The four S-parameters of the MODFETs were measured from 0.1 to 26.5 GHz at 300 K using a Hewlett-Packard 8510B network analyzer and a Cascade Microtech probe station. We transform the S parameters into Y parameters and extract values for the equivalent circuit model elements: extrinsic transconductance at high frequencies g_m (rf), gate-source capacitance C_{gs}, and gate-drain capacitance C_{gd}.[8] Table II gives these element values versus d_{chan}. With increasing d_{chan} significant effects are: the increase of the g_m (rf) and the increase in the value of C_{gd}, an undesirable feedback element which may increase because of the thinner depletion width associated with the smaller band gap of the higher In content channel. Also, note the lower value of the g_m (dc) compared to the g_m (rf) especially for $d_{\text{chan}} = 0$. This difference is associated with electron traps which respond at low frequency[9] and therefore the closer agreement between the rf and dc g_m for $d_{\text{chan}} = 30$ nm may indicate a sharp reduction of traps for graded pseudomorphic layers. The reason for this may be that the larger conduction band offset shifts the trap energy making occupation energetically unfavorable, or the layer strain may cause a reduction in the trap density. This effect is under investigation.

From the S parameters, we determine current gain h_{21}, and the maximum unilateral power gain G_u, which are plotted versus frequency in Fig. 3 for our best device having $d_{\text{chan}} = 30$ nm. We see that h_{21} rollsoff at -6 dB/octave and extrapolates to a cutoff frequency $f_T = 120$ GHz. The best values of f_T versus d_{chan} are given in Table II. G_u rolls off at -6 dB/octave and extrapolates to a cutoff frequency of $f_{\max}$. Values of $f_{\max}$ are given in Table II. $f_{\max}$ is affected by extrinsic elements such as gate resistance and capacitance and is not simply related to the carrier transit time.

TABLE III. Effective electron velocities v_{eff} calculated from measured values of cutoff frequency f_T and from dc value of g_m vs channel thickness d_{chan} for MODFET having $L_G = 0.25$ μm.

d_{chan} (nm)	$V_{\text{eff}}(f_T)$ (cm/s)	$V_{\text{eff}}(g_m)$ (cm/s)
0	1.57×10^7	9.19×10^6
20	1.67×10^7	1.58×10^7
30	1.88×10^7	1.92×10^7

The current gain cutoff frequency is determined by the transit time of carriers under the gate and is given by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{v_{\text{eff}}}{2\pi L_g}, \qquad (2)$$

where v_{eff} is the effective drift velocity of electrons in the InGaAs channel. Equation (2) provides two ways to determine v_{eff}; from the measured f_T, and from the measured g_m (dc). Values for v_{eff} from both these methods are given in Table III and are in close agreement. Both methods show that v_{eff} increases significantly with d_{chan}, and does not depend on only the endpoint In mole fractions.

V. CONCLUSIONS

We have demonstrated that composition grading by variation of MBE effusion cell temperature can be conveniently achieved and produce high performance pseudomorphic MODFETs. For In mole fraction $x = 0.65$, no misfit dislocations are produced up to a thickness of 30 nm, consistent with the BVM theory of lattice strain. MODFETs having gate lengths of $L_g = 0.25$ μm were fabricated and the best devices have dc extrinsic transconductance $g_m = 720$ mS/mm and current gain cutoff frequency $f_T = 120$ GHz; excellent values for MODFETs of this gate length. The improvement in device performance is ascribed to the high In context $x = 0.65$ at the heterointerface and also to the thickness of the graded channel.

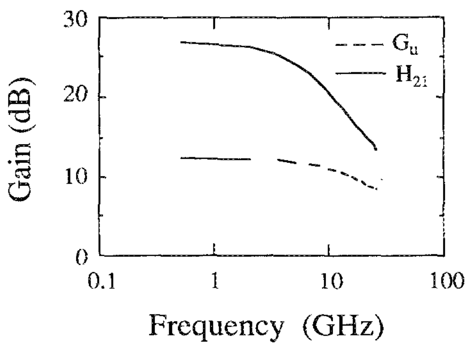

FIG. 3. Current gain h_{21} and unilateral gain G_u from S-parameter measurements for best pseudomorphic InAlAs/InGaAs/InP MODFET with $d_{\text{chan}} = 30$ nm and with $L_G = 0.25$ μm. Extrapolations to 0 dB axis give $f_T = 120$ GHz and $f_{\max} = 100$ GHz at 300 K.

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