Reduced lattice temperature high-speed operation of pseudomorphic InGaAs/GaAs field-effect transistors

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This letter presents a detailed study of the temperature dependence of submicron pseudomorphic InGaAs on GaAs substrate modulation doped field-effect transistors (MODFETs), doped-channel metal insulator field effect transistors (MISFETs), and metal semiconductor field-effect transistors (MESFETs). We determine similar variation in [redacted] these different pseudomorphic InGaAs/GaAs field-effect transistors provide similar potential for high-speed operation.

The advent of a reproducible cryogenic microwave measurement system[1] has allowed for detailed studies of the reduced lattice temperature operation of pseudomorphic InGaAs/GaAs field-effect transistors (FETs). Recent results include cryogenic high-speed measurements of doped channel metal insulator field-effect transistors (MISFETs),[2] modulation doped field effect transistors (MODFETs),[3] and metal semiconductor field-effect transistors (MESFETs).[4,5] The MODFET is attractive for the enhanced electron mobility achieved by reduced ionized [redacted] MISFET is distinguished by a narrow-gap active channel and undoped wide-gap insulator, which is opposite to the MODFET doping scheme. The advantages of this device design includes higher current drivability and higher breakdown voltage. The MESFET is attractive since do- [redacted] gate lengths from 1.0 to 0.1 μm.[6] The recent results in the literature raises the question of how significant are the contributions of high-electron mobility and two-dimensional electron transport in the high-speed operation of InGaAs/GaAs FET performance.

strate MODFETs, doped-channel MISFETs, and MESFETs. We determined similar increases in the measured extrinsic F_T and similar dependances of the effective electron velocity, v_{eff}, with reduced lattice temperature for the different FETs.

The MODFET structure used in this study was grown by solid-source molecular beam epitaxy (MBE) and consists of a 1 μm GaAs buffer, 170 Å $In_{0.2}Ga_{0.8}As$ strained channel, 50 Å undoped $Al_{0.25}Ga_{0.75}As$ undoped spacer, δ-doped Si plane with areal density 7×10^{12} cm^{-2}, 350 Å undoped $Al_{0.25}Ga_{0.75}As$ insulator, and a 200 Å cap layer of n-GaAs Si doped to 2.7×10^{18} cm^{-3}. The MESFET was grown by metalorganic chemical vapor deposition and consists of an undoped 600 Å $In_{0.18}Ga_{0.82}As$ layer, and an undoped 1000-Å-thick layer of $In_yGa_{1-y}As$ with the In composition graded from 0.18 to 0 at the surface for an [redacted] cles and subsequent capless annealing at 850 °C for 20 min. The peak carrier concentration in the channel is 2×10^{18} cm^{-3}. The doped channel MISFET was grown by solid source MBE and consists of a 1 μm GaAs buffer, 150 Å $In_{0.3}Ga_{0.7}As$ strained channel Si doped to 3×10^{18} cm^{-3}, 250 Å undoped $Al_{0.35}Ga_{0.65}As$ insulator, and a 200 Å cap [redacted] wet chemical etching. The MESFETs in this study have gate dimensions of 0.25×200 μm and 0.5×200 μm with a source-drain spacing of 2 μm. The MODFETs have gate dimensions of 0.35×100 μm and 0.47×100 μm with a source-drain spacing of 1 μm. The MISFETs have gate [redacted]

S-parameter data was collected from 0.5 to 26.5 GHz using a Hewlett-Packard 8510 B network analyzer. Measurements have been made at a temperature of 300 K using a Cascade model 42 D high-frequency probe station and at 110 K using a custom-built cryogenic high-frequency probe station.[1] Calibrations were performed "off-water" using an impedance standard substrate from Cascade Microtech. The measured s parameters are used to calculate the h parameters. In Fig. 1, we plot typical $|h_{21}|$ versus

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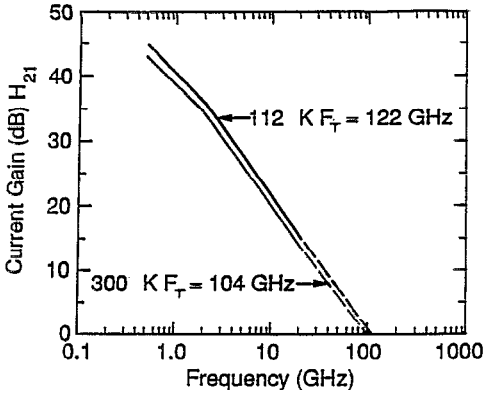

FIG. 1. Plot of the forward short-circuit current gain h_{21} vs frequency at 300 and 112 K for a $In_yGa_{1-y}As$ graded channel MESFET (Ref. 4). The gate dimensions are 0.25×200 μm and the F_T increases from 104 to 122 GHz when the lattice temperature is reduced from 300 to 112 K.

frequency results for a 0.25×200 μm InGaAs/GaAs MESFET at 300 and 112 K. We observe no evidence of resonance or inductive effects and the current gain follows a -6 dB/octave roll-off which extrapolates to the unity

sured peak F_T improves from 104 to 122 GHz when the lattice temperature is reduced from 300 to 112 K.

In Fig. 2, we plot the typical percentage change from 300 to 110 K in the extrinsic F_T for the three FET structures for gate lengths between 0.5 and 0.25 μm. When the effect of pad parasitics is removed the percentage increase in F_T is less than 30% for all devices. The peak F_T at 300

A detailed analysis of the extrinsic s parameters has been made to extract the intrinsic device parameters. It is important to extract the intrinsic device parameters to accurately measure the trends of important physical parameters for different device structures and different lattice temperatures. The hybrid-π equivalent circuit of Fig. 3 was used to fit the measured s parameters. The circuit analysis technique originally proposed in Ref. 7 is used to help to

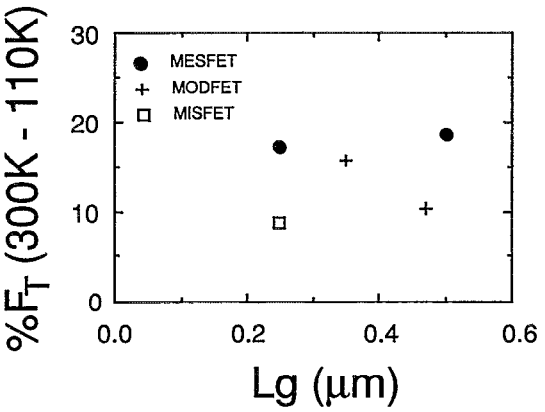

FIG. 2. Plot of the typical percentage increase in the measured F_T vs gate length for the InGaAs/Gas MODFETs, doped channel MISFETs, and MESFETs studied.

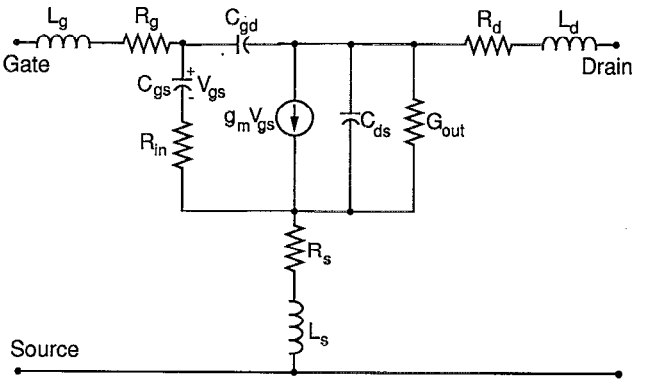

FIG. 3. Schematic of the hybrid-π circuit model used to fit the measured s parameters and validate the extracted small-signal circuit element values.

uniquely identify the small-signal element values. The pad parasitics were determined by measuring a gateless device with the technique outlined in.[8]

Once the small-signal element values have been determined and the values validated by fitting to the equivalent

v_{eff}, from:

$$v_{\text{eff}} = L_g \frac{g_m}{C_{gs} + C_{dg}}. \tag{1}$$

The v_{eff} is then plotted versus temperature in Fig. 4. Hall-

when the lattice temperature is reduced from 300 to 77 K. The electron mobility decreases by 2% in the doped channel MISFET and decreases by 7% in the MESFET. Independent determination for 5% indium channel MODFETs have shown a saturated velocity increase of 20% when the lattice temperature is reduced from 300 to 100 K.[9] These results are important for they provide direct experimental evidence that the low-field electron mobility is not the dominant factor in determining the high-speed performance of InGaAs/GaAs FETs. Similar conclusions about

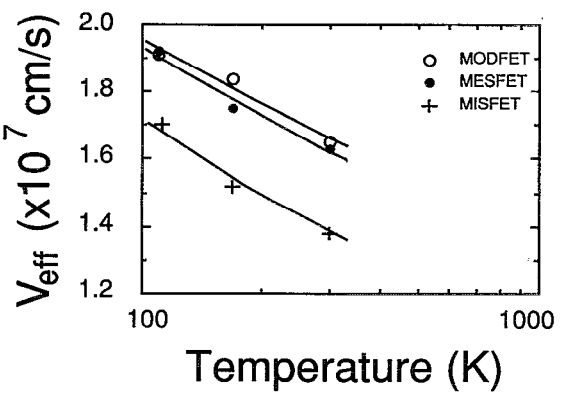

FIG. 4. Plot of the extracted effective electron velocity, v_{eff}, vs L_g for the InGaAs/GaAs FETs studied. The $v_{\text{eff}} \sim T^{-b}$ where $0.15 < b < 0.20$ over the temperature range of 300 to 110 K.

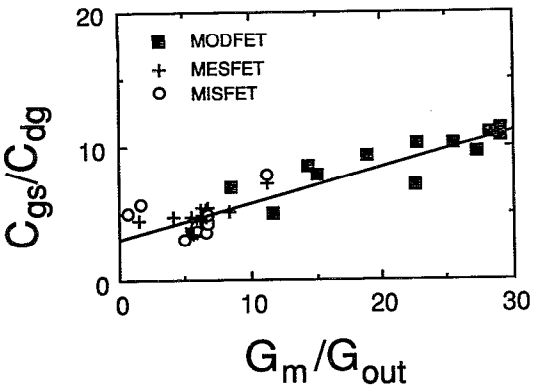

FIG. 5. Plot of the ratio of C_{gs}/C_{gd} vs g_m/g_{out} for all InGaAs/GaAs FETs measured in this study. The data include results over the temperature range of 300–110 K. The measured data fit well to a slope, β, of -0.27 which agrees well with 300 K results reported in Ref. 11.

the relevance of electron mobility for high-speed performance have been drawn from recent results in the literature.[4,10]

To gain insight into the physical mechanisms controlling high-speed operation we have applied a feedback correlation analysis as originally proposed in Ref. 11:

$$C_{gs}/C_{gd}=1+\beta g_m/g_{out} \tag{2}$$

where C_{gs} is the gate-source capacitance, C_{gd} is the drain-gate capacitance, g_m is the transconductance, g_{out} is the output conductance, and β is an empirical fitting parameter. We can determine the parameter β by plotting C_{gs}/C_{gd} versus g_m/g_{out}. Since g_{out} increases as current spreads out of the conducting channel, and g_m represents control of the channel current, the ratio g_m/g_{out} is a measure of the confinement of rf current. A small value of β results in a large g_m/g_{out} ratio reflecting good current confinement in the drift region of the device (high-voltage gain and small output conductance).

In Fig. 5 we plot C_{gs}/C_{gd} versus g_m/g_{out} for the three different FETS for several different devices over a temperature range from 300 to 110 K. We find $\beta=0.27$ for all the devices over the temperature range 300 to 100 K which agrees quite well with the value of $\beta\sim0.3$ extracted in Ref. 11 for 300 K measurements. This analysis not only confirms the previous trends observed in the literature[4] but also reveals that there is no enhanced carrier confinement under high fields at reduced lattice temperatures for these InGaAs/GaAs FETs.

In conclusion, based on detailed cryogenic microwave measurements of pseudomorphic InGaAs/GaAs MODFETs, doped channel MISFETs, and MESFETs we find a similar variation of v_{eff} with temperature. Because of the high-electric fields associated with submicron FET operation the saturated velocity of electrons in the gate-drain portion of the transistor is the most important parameter for high-speed operation. We find no evidence of enhanced carrier confinement in either reduced lattice temperature operation or in the two-dimensional quantum well structures. These results provide direct experimental evidence that with proper device design these different pseudomorphic InGaAs/GaAs FET structures all provide good potential for high-speed operation.

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