# **Briefs**

# DC and RF Characterization of Short-Gate-Length InGaAs/InAlAs MODFET's

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Abstract-Lattice-matched InGaAs/InAlAs MODFET's with gate lengths down to 0.15  $\mu m$  have been fabricated and characterized. A large discrepancy is found between the  $g_m$  measured at dc and microwave frequencies and is attributed to the finite time constant of electron emission from deep traps in the InAlAs. A maximum  $f_T$  of 112 GHz is measured on a 0.15-µm gate-length device. Devices with more shallow recessed gates are found to have a 50-percent larger output conductance that causes the devices to exhibit an  $f_T$  that is greater than  $f_{\max}$ .

## I. Introduction

The InGaAs/InAlAs modulation-doped field-effect transistor (MODFET) has many advantages over the conventional GaAs/AlGaAs MODFET, including larger electron sheet carrier concentrations [1], higher electron mobilities and saturation velocities in the InGaAs channel [2], [3], and with bandgaps of 0.75 and 1.53 eV, respectively (corresponding to wavelengths of 1.65 and  $0.70 \mu m$ , respectively), these materials are prime candidates for integration with long-wavelength optical devices. In order to determine the ultimate device performance of this material system, however, the effect of growth- and fabrication-related parameters must be assessed. The gate recess depth is one such important parameter that can be controlled by fabrication. In this brief we report the effect of gate recess depth on the dc and microwave performance of InGaAs/InAlAs MODFET's.

# II. DEVICE STRUCTURE AND FABRICATION

The In<sub>0.53</sub>Ga<sub>0.47</sub>As/In<sub>0.52</sub>Al<sub>0.48</sub>As lattice-matched MODFET used in this study was grown by molecular-beam epitaxy on semiinsulating InP. The structure consists of a 0.25-µm InAlAs buffer layer, 500-Å undoped InGaAs channel layer, 300-Å n<sup>+</sup>-InAlAs donor layer, and 300-Å undoped InAlAs Schottky layer. Finally, a 200-Å undoped InGaAs cap layer was included to reduce gate capacitance and gate leakage [4]. However, this has not yet been substantiated on our devices. Hall measurements showed a sheet carrier concentration and mobility of  $2.4 \times 10^{12}$  cm<sup>-2</sup> and  $10\ 005$ cm<sup>2</sup>/V-s, respectively, at 300 K.

Device fabrication began with mesa isolation and ohmic contact deposition using standard photolithography and liftoff processing. Ohmic contacts of AuGe/Ni/Au exhibited good surface morphol-

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ogy with a typical transfer resistance of 0.35  $\Omega$ -mm. Center-fed 100- $\mu$ m-wide gates with gate lengths ranging from 0.15 to 0.3  $\mu$ m were defined by electron-beam lithography using a Cambridge 6.5 EBMF system. A bilayer resist scheme consisting of 1000 Å of 950K PMMA on top of 4000-Å 496K PMMA was used. Following a brief oxygen plasma descum, gates were recess etched in H<sub>3</sub>PO<sub>4</sub>: H<sub>2</sub>O<sub>2</sub>: H<sub>2</sub>O (1:1:38) until a predefined "gateless" saturation current was obtained. Different gate recess times were used on the two separate device fabrication runs (A and B). Run A was etched for 22 s giving a gateless current of 440 mA/mm and run B was etched for 25 s giving a gateless current of 260 mA/mm, as measured on 1-µm source-drain spaced devices. The recess trench width is slightly larger than the actual gate length due to lateral etching and is approximately the same width in both runs A and B.

## III. RESULTS

The dc characteristics of the devices were measured using an HP4145 semiconductor parameter analyzer. Peak extrinsic transconductances  $(g_m)$  as measured on 100- $\mu$ m-wide devices typically ranged from 300 to 450 mS/mm with a few devices above 500 mS/mm. The relatively large contact resistance due to the undoped cap contributed to these low transconductances. Threshold voltages of runs A and B were around -0.85 and -0.6 V, respectively. Fig. 1 shows the I-V and transfer characteristics of a  $0.15-\mu m$  gatelength InGaAs/InAlAs MODFET from run A. The I-V characteristic clearly shows a "kink," the origin of which has been attributed to traps in the InAlAs buffer or donor layers [5]. Below the kink, free electrons in the InAlAs or hot electrons that transfer from the InGaAs channel are captured by deep electron trapping centers in the InAlAs. Further increase in the drain bias raises the trapping centers above the Fermi level on the drain side of the gate whereby trapped electrons are emitted into the InGaAs channel. This increased electron concentration in the channel causes the rapid increase in drain current observed above the kink. Similarly the I-Vcharacteristics from run B (Fig. 2(a)) also have a "kink"; however, the dc output conductance is approximately 50 percent lower than the shallow etched run A.

Microwave measurements from 0.25 to 40 GHz were performed on 100-µm-wide devices using a Cascade Microtech probe station and an HP8510 network analyzer. The devices were biased for maximum gain as determined by monitoring  $S_{21}$ . The gate bias for maximum gain coincided with the point of maximum dc  $g_m$  for run A (Fig. 1(b)) while for run B the gate bias is in a region beyond the peak  $g_m$  (Fig. 2(b)) where  $g_m$  falls below 150 mS/mm. A closer look at the dc transfer characteristic indicates that the microwave bias point is at the approximate peak of the second  $g_m$  hump, which is clearly visible on run A and is just barely visible on run B. The RF extrinsic  $g_m$  (as determined from  $y_{21}$ ) measured at this bias point ranged from 550 to 650 mS/mm for both runs A and B. We attribute this large discrepancy between dc and RF  $g_m$  to frequencydependent parasitic charge fluctuation in the InAlAs. Charge fluctuations due to deep traps, free-electron generation, and neutralization of donors are all mechanisms that degrade the dc  $g_m$  and are time dependent in nature [6]. The frequency-dependent effects on  $g_m$  of the latter two mechanisms has not as yet been observed and may only be negligible at very high frequencies. The finite electron capture and emission time constant of deep traps is the likely mechanism for the large frequency-dependent  $g_m$  especially in view of

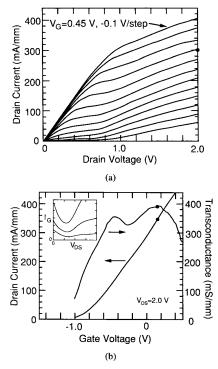


Fig. 1. (a) I-V and (b) transfer characteristics of an  $0.15-\mu m$  gate-length InGaAs/InAlAs MODFET from run A. Microwave bias point for maximum gain is indicated. The inset shows a negative diode impedance from gate to drain at high drain and gate bias for run A that is evidence of an increase in hot-electron transfer into the InAlAs (horiz.: 0.5 V/div., vert.: 0.01 mA/div., top:  $V_G = 0.65 \text{ V}$ , -0.1 V/step).

their noticeable effect on the I-V "kink." An emission time constant of about 2 ms is estimated for at least one trap level found in InAlAs [7]. At microwave frequencies, captured electrons can be considered "frozen" in traps and are not modulated by the gate with the result that  $g_m$  is not reduced. The second hump in the  $g_m$  likely arises as deep traps become completely filled causing the  $g_m$  to again increase. The relative size of the second hump depends on the separation between the quasi-Fermi level and the trap levels in the InAlAs. A more detailed study of this phenomenon is currently under investigation.

Short-circuit current-gain cutoff frequency  $f_T$  and unilateral power-gain cutoff frequency  $f_{\text{max}}$  are found by extrapolating to unity gain. No corrections were made to account for pad parasitics. All our data strongly reflect a -6-dB/octave rolloff as substantiated by Ka-band (27-40 GHz) measurements (see Fig. 3) and indicates the absence of any abnormally large gate capacitance, which has been attributed to cause the -12-dB/octave rolloff observed in the unilateral power gain at cryogenic temperatures [8].  $f_T$ 's of 112 and 100 GHz were measured for the 0.15-µm gate-length device of run A and 0.19- $\mu$ m gate-length device of run B, respectively. The  $f_{\rm max}$ of run A, however, is 98 GHz, which is less than the  $f_T$ . The  $f_{\text{max}}$ obtained from run B is 125 GHz, which is among the highest reported to date [9], [10] and is much higher than  $f_T$ . The only significant process difference is that run A was etched less than run B and, as mentioned above, resulted in run A having a 50-percent higher output conductance (both dc and RF) than run B. This "crossover" in the  $f_{\text{max}}$  and  $f_T$  can be attributed to the large RF output conductance  $(g_0)$  of devices from run A. An exact solution of the equivalent circuit model for  $f_T$  and  $f_{\text{max}}$  shows that, as  $g_0$ increases from 30 mS/mm (run B) to 45 mS/mm (run A),  $f_{\text{max}}$ decreases much more rapidly than  $f_T$  and a crossover point is

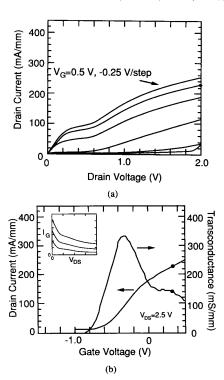


Fig. 2. (a) I-V and (b) transfer characteristics of a  $0.19-\mu m$  gate-length InGaAs/InAlAs MODFET from run B. Microwave bias point for maximum gain is indicated. The inset shows the absence of a negative diode impedance from gate to drain for run B (Horiz.: 0.5 V/div., vert.: 0.5 mA/div., top:  $V_G = 0.6 \text{ V}$ , -0.1 V/step).

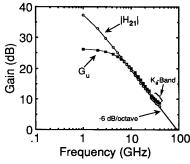


Fig. 3. The measured short-circuit current gain  $|h_{21}|$  and maximum unilateral gain  $G_u$  versus frequency for a  $0.21 + \mu m$  device of run B is extrapolated to unity to obtain  $f_T$  and  $f_{\max}$ , respectively. Data strongly indicate a -6-dB/octave rolloff at least out to the maximum measurement frequency of 40 GHz (Ka-band).

reached where  $f_T$  is larger than  $f_{\rm max}$ . The exact  $g_0$  where this crossover takes place depends on the other element values of the equivalent circuit but indicates that both  $f_T$  and  $f_{\rm max}$  should be stated for a more complete description of the device.

The larger RF  $g_0$  of run A does not appear to be related to deep traps because traps are too slow to respond at high frequencies. This frequency dependence, which has also been observed in InAlAs/InGaAs heterojunction MESFET's [11], is demonstrated by the fact that  $g_0$  derived from microwave measurements is about 1.5 times smaller than the dc value. A lack of sufficient carrier confinement in run A, due perhaps to the transfer of hot electrons

from the InGaAs channel into the InAlAs layers, may account for the higher  $g_0$ . An "excess" gate current and negative diode impedance from the gate to the drain has been attributed to the collection by the gate of such hot transferred electrons [12]. The inset in Fig. 1(b) of run A clearly shows a negative impedance at high gate and drain bias while the inset in Fig. 2(b) of run B shows no such effect. This is further supported by microwave measurements of the real part of  $y_{12}$  where we have also found a negative diode impedance only for devices from run A [12].

## IV. CONCLUSION

We have fabricated InGaAs/InAlAs MODFET's on InP with various gate lengths down to 0.15  $\mu$ m. A large discrepancy between transconductance measured at dc and microwave frequencies has been found and is attributed to the finite time constant of deep traps in the InAlAs layers. The sensitivity of device characteristics to gate recess depth has been demonstrated. Devices with a shallow gate recess show a 50-percent larger output conductance and leads to a "crossover" in the  $f_T$  and  $f_{\rm max}$  cutoff frequencies. Such shallow etched samples exhibit an  $f_T$  larger than  $f_{\rm max}$ . Evidence for the transfer of hot electrons into the InAlAs layers was found for the shallow etched sample, which may explain the larger output conductance.

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## REFERENCES

- [1] A. S. Brown, U. K. Mishra, J. A. Henige, and M. J. Delaney, "The impact of epitaxial layer design and quality on GaInAs/AlInAs high-electron-mobility transistor performance," J. Vac. Sci. Technol. B., vol. 6, pp. 678-681, Mar./Apr. 1988.
- [2] K. Onabe, Y. Tashiro, and Y. Ide, "High-mobility two-dimensional electron gas in modulation-doped InAlAs/InGaAs heterostructure," Surface Sci., vol. 174, pp. 401-407, 1986.
- [3] A. Cappy, B. Carnez, R. Fauquembergues, G. Salmer, and E. Constan, "Comparative potential performance of Si, GaAs, GalnAs, InAs, submicrometer-gate FET's," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 2158-2160, Nov. 1980.
- [4] H. Hida, K. Ohata, Y. Suzuki, and H. Toyoshima, "A new low-noise AlGaAs/GaAs 2DEG FET with a surface undoped layer," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 601-607, May 1986.
- [5] A. S. Brown et al. in Proc. Int. Conf. GaAs and Related Compounds, 1988.
- [6] F. Ponse, W. T. Masselink, and H. Morkoç, "Quasi-Fermi level bending in MODFET's and its effect on FET transfer characteristics," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1017-1023, June 1985.
- [7] K. Nakashima, S. Nojima, Y. Kawamura, and H. Asahi, "Deep electron trapping centers in Si-doped InAlAs grown by molecular beam epitaxy," Phys. Status Solidi (a), vol. 103, pp. 511-516, 1987.
- [8] J. Kolodzey et al., "Frequency response of AlInAs/GaInAs/InP modulation-doped field effect transistors at cryogenic temperature," in Device Research Conf. Tech. Dig., June 1988, paper IIIB-7; also in IEEE Trans. Electron Devices, vol. 35, p. 2442, Dec. 1988.
- [9] L. D. Nguyen, D. C. Radulescu, P. J. Tasker, W. J. Schaff, and L. F. Eastman," 0.2 

  µm gate-length atomic-planar doped pseudomorphic Al<sub>0.3</sub>Ga<sub>0.7</sub>As/In<sub>0.25</sub>Ga<sub>0.75</sub>As MODFET's with f<sub>T</sub> over 120 GHz," IEEE Electron Device Lett., vol. 9, pp. 374-376, Aug. 1988.
- [10] L. Lester, R. Tiberio, and E. Wolf, "0.15  $\mu$ m gate-length double recess pseudomorphic HEMT with  $F_{\rm max}$  of 350 GHz," presented at the IEDM, San Francisco, Dec. 1988.
- [11] J. B. Kuang et al., "Kink effect in submicrometer-gate MBE-grown InAlAs/InGaAs/InAlAs heterojunction MESFET's," IEEE Electron Device Lett., vol. 9, pp. 630-632, Dec. 1988.
  [12] L. F. Palmateer et al., "Observation of excess gate current due to
- [12] L. F. Palmateer et al., "Observation of excess gate current due to hot electrons in 0.2 μm gate length, 100 GHz f<sub>T</sub> AlInAs/GaInAs/InP MODFET's," Proc. Int. Conf. GaAs and Related Compounds, 1988.

# Si/SiGe Heterojunction Bipolar Transistor Made by Molecular-Beam Epitaxy

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Abstract—Si/SiGe heterostructure bipolar transistors (HBT's) were fabricated and compared to Si homojunction transistors with similar doping levels. Low-temperature Si-MBE was used to form the heterojunction and the homojunction layer sequences. A wet chemical selective etching technique was used for the first time to contact the thin (80 nm) base layer of the heterojunction transistor. A peak current gain of 200 to 400 was measured for the heterostructure devices, compared to a gain of two for the homojunction structure. The current gain current dependence of the heterostructure devices could be attributed to surface recombination effects.

## I. Introduction

Heterojunction bipolar transistors (HBT's) show great potential for future digital and microwave applications. Impressive results have been achieved in the III-V semiconductor system [1], [2]. HBT's provide a higher energy barrier  $\Delta E_v$  to holes injected from the p-base into the n-emitter as compared to the injection of electrons into the base. Different approaches have been reported in the past to transfer the heterojunction principle to the silicon system. One approach is to use amorphous silicon or microcrystalline silicon emitters [3]. Another solution, sometimes called a pseudo-heterojunction, utilizes the presence of thin interface oxide between the base and the polysilicon emitter. The back injection of holes is limited by tunneling through the thin oxide barrier [4]. However, the interface state density, and difficulty in controlling the oxide barrier thickness.

Recent progress in the MBE growth of strained SiGe on Si has allowed bandgap engineering to be transferred to the silicon-based system [5]. Due to the lower bandgap of the SiGe alloy in the base, the emitter injection efficiency of the transistor is improved and is less dependent on the doping levels in the emitter and the base. This provides a new design flexibility in choosing the doping level ratio. A high base doping concentration leads to many advantages, such as low base resistance, low noise figure, and high current drive capability for the transistor. Base doping concentrations as high as  $2 \times 10^{20}$  cm<sup>-3</sup> have been reported for GaAs HBT's [6]. A low emitter doping concentration produces a small emitter junction capacitance and consequently a high cutoff frequency and a high emitter breakdown voltage. The implementation of heterojunction in the silicon material system will further extend the high-speed performance of Si bipolar technology.

## II. THE Si/SiGe HETEROSYSTEM

A characteristic feature of the Si/SiGe heterosystem is the large mismatch in the lattice constants. This mismatch produces strain, which strongly influences the band structure. When SiGe is grown onto a Si substrate (Si is unstrained, SiGe is fully compressed), the difference in the bandgap is accommodated by a difference in the valence band  $\Delta E_v$ , resulting in the ideal situation for a hetero bipolar junction [11]. However, the energy gap difference does not necessarily mean that a high current gain can be obtained. It simply means that the hole injection current becomes a negligible part of the base current compared to the base recombination current and the recombination current at the interface. To have a useful tran-

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