Agenda

- Quad-Core AMD Opteron™
- Long Term Roadmap
- AMD HPC WW
Agenda

- **Quad-Core AMD Opteron™**
  - Architecture
  - Benchmarks
  - Tools
- Long Term Roadmap
- AMD HPC WW
Quad-Core AMD Opteron™ Processors

More than just four cores
- Significant CPU Core Enhancements
- Significant Cache Enhancements

World-class performance
- **Native Quad Core**
  - Faster data sharing between cores
- **Enhanced AMD-V™**
  - Nested paging acceleration for virtual environments

Reducing total cost of ownership
- **Performance/Watt** leadership
  - Consistent 95W thermal design point
  - Low power 68W solutions
- **Drop-in upgrade**
  - Socket F compatibility – BIOS upgrade
  - Leverage existing platform infrastructure
- **Common Core Architecture**
  - One core technology top-to-bottom
  - Top-to-bottom platform feature consistency
AMD Quad-Core Processor

The Die

Comprehensive Upgrades for SSE128
Can quadruple floating-point capabilities

New Highly Efficient Cache Structure with Shared L3 Cache
Balance of dedicated and shared cache for optimum quad-core performance

CPU Core Enhancements
To benefit applications by improving overall efficiency and performance of cores

Virtualization Enhancements
New "Nested Paging" feature designed for near native performance on virtualization applications

Advanced Power Management
Provides granular power management resulting in improved power efficiency

DRAM Controller Enhancements
To improve overall memory performance with native quad-core processing

Quad-Core AMD Opteron™ Processor Design for Socket F (1207)

HyperTransport™ technology links provide up to 24 GB/s peak bandwidth per processor.

10.7GB/s @ DDR2-667
128-bit SSE and 128-bit Loads

Comprehensive set of upgrades for improved performance on floating point- and graphics-intensive applications

Double vector SSE performance
Both SSE Floating-point and SSE Packed Integer
Avoid creating bottlenecks in instruction or data delivery
### Comprehensive Enhancements for SSE128

**AMD Dual-Core Opteron™ versus Quad-Core Opteron™**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AMD Opteron™ with DDR2</th>
<th>Quad-Core AMD Opteron™</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSE Exec Width</td>
<td>64</td>
<td>128 + SSE MOVs</td>
</tr>
<tr>
<td>Instruction Fetch BW</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle + Unaligned Ld-Ops</td>
</tr>
<tr>
<td>Data Cache Bandwidth</td>
<td>2 x 64bit loads/cycle</td>
<td>2 x 128bit loads/cycle</td>
</tr>
<tr>
<td>L2/NB Bandwidth</td>
<td>64 bits/cycle</td>
<td>128 bits/cycle</td>
</tr>
<tr>
<td>FP Schedule Depth</td>
<td>36 Dedicated x 64-bit ops</td>
<td>36 Dedicated x 128-bit ops</td>
</tr>
</tbody>
</table>

**Can perform SSE MOVs in the FP “store” pipe**
- Execute two generic SSE ops+SSE MOV each cycle (+two 128-bit SSE loads)

**SSE Unaligned Load-Execute mode**
- Reduce alignment requirements for SSE ld-op instructions
- Minimize awkward pairs of separate load and compute instructions
- To improve instruction packing and decoding efficiency
‘Barcelona’ ... Not Just Four Cores

Comprehensive 128-bit SSE Upgrades

**Goal: Balanced SSE Execution**

<table>
<thead>
<tr>
<th></th>
<th>Intel Clovertown</th>
<th>AMD Barcelona</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>64-bit Platforms</strong></td>
<td>1x</td>
<td>2x</td>
</tr>
<tr>
<td><strong>Instruction Fetch Bandwidth</strong></td>
<td>1x</td>
<td>1x</td>
</tr>
<tr>
<td><strong>Data Cache Bandwidth</strong></td>
<td>1x</td>
<td>1x</td>
</tr>
<tr>
<td><strong>L2 Cache / North-Bridge Bandwidth</strong></td>
<td>1x</td>
<td>2x</td>
</tr>
</tbody>
</table>

- Barcelona **doubles** Instruction and Data pipelines ... Intel’s pipeline doesn’t
  - Helps keep 128-bit SSE pipeline full for optimum performance
- Dedicated 36-entry floating-point scheduler can reduce application latency
  - Intel 32-entry scheduler shared between floating-point and integer operations
- Incredible performance boost, **per core**, on target applications!
Balanced, Highly Efficient Cache Structure

**Dedicated L1**
- AMD’s 64KB/64KB vs. Intel’s 32KB/32KB
- Allows 2 loads per cycle

*Handle Data Quickly and Efficiently.*

**Dedicated L2**
- Dedicated cache to eliminate conflicts of shared caches
- Designed for true working data sets

*Avoid Thrashing. Minimize Latency.*

**Shared L3 - New**
- Designed for optimum memory use and allocation for multi-core
- Ready for expansion at the right time for customers

*Reduces Latency to Main Memory.*

Efficient memory handling reduces need for “brute force” cache sizes

Core 1
- Cache Control
- 64KB

Core 2
- Cache Control
- 64KB

Core 3
- Cache Control
- 64KB

Core 4
- Cache Control
- 64KB

2MB+

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# Barcelona Enhancements

## CPU Core IPC Enhancements

- Advanced branch prediction
- 32B instruction fetch
- Sideband Stack Optimizer
- Out-of-order load execution
- TLB Optimizations (1G pages)
- Data-dependent divide latency
- More Fastpath instructions
  - CALL and RET-Imm instructions
  - Data movement between FP & INT
- Bit Manipulation extensions
  - LZCNT/POPCNT
- SSE extensions
  - EXTRQ/INSERTQ,
  - MOVNTSD/MOVNTSS

## Deliver more DRAM bandwidth

- Independent DRAM controllers
- Optimized DRAM paging
- Re-architect NB for higher BW
- Write bursting
- DRAM prefetcher
- Core prefetchers

## Balanced, Highly Efficient Cache Structure

- Doubled L1 cache bandwidth & Ins. Decode
- Dedicated 512KB L2 cache
- Shared L3 cache
Improving Processor Power Management with AMD PowerNow!™ Technology enhancements

**Dual-Core**

- **CORE 0**: 75% utilization at 35 MHz
- **CORE 1**: 35% utilization at 75 MHz

MHz and voltage is locked to highest utilized core’s p-state

**Native Quad-Core**

- **CORE 0**: 75% utilization at 35 MHz
- **CORE 1**: 35% utilization at 75 MHz
- **CORE 2**: 10% utilization at 1 MHz
- **CORE 3**: 1% utilization at 1 MHz

MHz is independently adjusted separately per core. Voltage is locked to highest utilized core’s p-state

Native Quad-Core technology enables enhanced power management across all four cores

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AMD CoolCore™ Technology
Turns off Blocks of CPU When Not in Use

Coarse Control (Core)
• Ex, FPU (hottest part of die)

Fine Control (Core)
• Incrementally Smaller Sections

Memory Controller
• Reads (turn off write logic)
• Writes (turn off read logic)

Example only: does not reflect actual areas of clock gating

AMD CoolCore™ is Automatic – No Drivers Needed!
Introducing Average CPU Power

**Average CPU Power (ACP)** - Measuring processor power draw on all CPU power rails while running accurate and relevant commercially useful high utilization workloads*

<table>
<thead>
<tr>
<th>ACP</th>
<th>TDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>105W</td>
<td>120W</td>
</tr>
<tr>
<td>75W</td>
<td>95W</td>
</tr>
<tr>
<td>55W</td>
<td>68W</td>
</tr>
</tbody>
</table>

Each ACP value includes power for Cores, Memory Controller, and HyperTransport™ links

ACP values are considerably lower than TDP
- Because AMD’s TDP values are conservative engineering design limits
- ACP includes workloads such as TPC-C, SPECcpu2006, SPECjbb2005, STREAM

TDP will continue to be leveraged for engineering thermal design maximum limits

*See slide “Details around testing”

SPEC® and the benchmark names SPECcpu2006, SPECjbb2005 are registered trademarks of the Standard Performance Evaluation Corporation.
Dual Dynamic Power Management™ (DDPM)

Separate power planes for cores and memory controller for:

- **Optimum power consumption** - Enables cores to operate at reduced power consumption levels while memory controller continues to run at full speed

- **Increased performance** - Memory controller can operate at higher frequency for increased bandwidth and performance
Projected Infrastructure Impact of Quad-Core

7Kw Power Budget

- Second-Generation AMD Opteron™ processors with planned upgrade path to quad-core within existing power & thermal envelopes
- Clovertown raises power & thermal requirements within each power band
- Intel customers may be forced to choose between higher power & cooling costs or wasted rack space

<table>
<thead>
<tr>
<th>Pwr. Band</th>
<th>Intel TDP</th>
<th>AMD TDP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dual</td>
<td>%+</td>
</tr>
<tr>
<td>High</td>
<td>80W</td>
<td>50%</td>
</tr>
<tr>
<td>Std.</td>
<td>65W</td>
<td>23%</td>
</tr>
<tr>
<td>Low</td>
<td>40W</td>
<td>25%</td>
</tr>
</tbody>
</table>

AMD Opteron™ processors
Designed to maximize server density and minimize transitions

Intel Xeon
Can waste data center space and increase transition pain

Wattage based on 2P systems, 8 DIMMs, TDP wattage for ‘Dempsey’, ‘Woodcrest’ & ‘Clovertown’ is estimated based on current publicly available processor and chipset values, AMD estimates, and an incremental 100 watts for fans, storage, and power supply. (see, eg: [http://techreport.com/etc/2006q2/woodcrest/index.x7pq=2](http://techreport.com/etc/2006q2/woodcrest/index.x7pq=2) and is subject to change. The examples contained herein are intended for informational purposes only. Other factors will affect real-world power consumption.
Performance-Per-Watt Scalability

Consistent power and thermals help deliver better performance per watt.
### Quad-Core AMD Opteron™ Benchmarks

#### PROCESSOR PERFORMANCE BENCHMARKS

**SPECint_rate2006 Performance Scaling**

<table>
<thead>
<tr>
<th>Processor Configuration</th>
<th>SPECint_rate2006 Peak</th>
<th>SPECfp_rate2006 Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quad-Core AMD Opteron™ Processor Model 2350</td>
<td>64.3</td>
<td>60</td>
</tr>
<tr>
<td>Xeon E5345</td>
<td>58.8</td>
<td>48.75</td>
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<tr>
<td>Quad-Core AMD Opteron™ Processor Model 2350</td>
<td>60</td>
<td>48.75</td>
</tr>
<tr>
<td>Xeon E5345</td>
<td>46.2</td>
<td>48.75</td>
</tr>
</tbody>
</table>

SPEC and the benchmark name SPECint are registered trademarks of the Standard Performance Evaluation Corporation. Results for Quad-Core AMD Opteron processor Model 2350 and Xeon E5345 are under submission to SPEC as of September 09, 2007. For the latest SPECint_rate2006 results visit [http://www.spec.org/cpu2006/results/](http://www.spec.org/cpu2006/results/).
Quad-Core AMD Opteron™ Benchmarks
PROCESSOR PERFORMANCE BENCHMARKS – Floating Point

SPECfp_rate2006 2P Servers

SPECfp_rate2006 4P Servers

SPEC and the benchmark name SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. Competitive benchmark results stated above reflect results published on www.spec.org as of Sep 9, 2007. The comparison presented above is based on results for Quad-Core AMD Opteron processor Model 2360 SE under submission to SPEC as of Sep 9, 2007. For the latest results visit http://www.spec.org/cpu2006/results/
Quad-Core AMD Opteron™ Benchmarks
STREAM

Memory Bandwidth - STREAM

STREAM - Memory Bandwidth

<table>
<thead>
<tr>
<th>Sub-tests</th>
<th>MB/sec</th>
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<tbody>
<tr>
<td>Copy</td>
<td>284%</td>
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<tr>
<td>Scale</td>
<td>283%</td>
</tr>
<tr>
<td>Add</td>
<td>261%</td>
</tr>
<tr>
<td>Triad</td>
<td>261%</td>
</tr>
<tr>
<td>Average</td>
<td>289%</td>
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</table>

Quad-Core AMD Opteron™ processor
Model 2350 (2GHz)
Xeon 5345
Quad-Core AMD Opteron™ Benchmarks

SHARED MEMORY PARALLEL PROCESSING

SPEComp2001® Performance Scaling

SPEComp2001® Performance

SPEC and the benchmark name SPECONPM are registered trademarks of the Standard Performance Evaluation Corporation. Results for Quad-Core AMD Opteron processor Model 2350 and Xeon 5345 are under submission to SPEC as of September 7, 2007. For the latest SPEComp2001 results visit http://www.spec.org/omp/ results/
Quad-Core AMD Opteron™ Benchmarks

**FLUENT**

**FLUENT 6.4.3 Quad-Core x86 2P Servers - 8 cores**

- **Fluent Performance**
- **Fluent Speedup Performance**

**Fluent Performance per Energy Consumption**

---

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Quad-Core AMD Opteron™ Benchmarks
LS-DYNA

LS-DYNA mpp971s - Quad-Core x86 2P Server

LS-DYNA Cluster Performance

LS-DYNA Performance

http://www.amd.com/us-en/Processors/ProductInformation/0,,30_118_8796_8800,00.html
HPC Benchmarks in progress
O&G, CAE, FSI, EDA, LMS, G&D, S&E

<table>
<thead>
<tr>
<th>O&amp;G</th>
<th>CAE</th>
<th>EDA</th>
<th>LMS</th>
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<tbody>
<tr>
<td>LANDMARK</td>
<td>LSTC LS-DYNA</td>
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<td>GORDON RESEARCH</td>
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<td>ABAQUS EXPLICIT</td>
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<td>• AMBER</td>
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<td>• SPOTFIRE</td>
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</table>

Forbes.com
LARGEST COMPANIES IN THE WORLD
Global High Performers

2007 Worldwide High Performance Computing
Agenda

- Quad-Core AMD Opteron™
- Long Term Roadmap
- AMD HPC WW
Agenda

- Quad-Core AMD Opteron™
- Long Term Roadmap
  - CPU
  - GPU & Torrenza
  - Fusion
- AMD HPC WW
The Smarter Choice for IT

In 1999, AMD introduced a long-term solution that customers could grow with.

In 2003, AMD permanently changed the IT landscape with the intro of the AMD Opteron™ processor.

In 2005, AMD showed the industry how to make the transition from single-core to native dual-core.

In 2007, the launch of ‘Barcelona’ will have an even greater impact...
Server/Workstation Brand Positioning

**PERFORMANCE 4-WAY AND 8-WAY**

**AMD Opteron™ 800 Series & 8000 Series Processors**
- Designed for 4-way and 8-way Server solutions
- First and only native x86 dual-core solution for 4-way / 8-way computing

**PERFORMANCE 2-WAY**

**AMD Opteron™ 200 Series & 2000 Series Processors**
- Designed for 2-way Server / Workstation solutions
- First native x86 dual-core solution for 2-way computing

**PERFORMANCE 1-WAY**

**AMD Opteron™ 100 Series & 1000 Series Processors**
- Designed for 1-way Server / Workstation solutions
- First native x86 dual-core solution for 1-way computing

**AMD Opteron™ Processors for Servers and Workstations**

- Direct Connect Architecture eliminates the bottlenecks inherent in front-side bus architectures by directly connecting CPU’s, memory and I/O for reduced latency and optimized memory performance.
- AMD Opteron™ processors offer industry leading performance-per-watt and improved system efficiency and application performance.
- AMD PowerNow!™ technology with Optimized Power Management decreases overall system power consumption without compromising system performance.
Multi-Core Roadmap Directions: One Size Does Not Fit All

Database, Transaction Processing, Search
- Multiple simultaneous unrelated tasks/sessions
- More threads (inherently parallel)
- Integer intensive - moderate single thread performance
- Great for high core-count processors

Technical Computing, HPC, Financial Apps, Workstation
- One problem broken into multiple tasks
- Larger data sets
- Less threads
- Floating point intensive - high single thread performance
- Great for low core-count, high frequency processors

Just adding more cores does not address all workloads
Workload Oriented Roadmap

Core-count
- Many cores: highly threaded apps
- Few cores: compute-intensive apps

Heterogeneous multiprocessing
- Optimize performance/Watt with workload accelerators
- Extending beyond basic core/frequency combinations
  - General purpose AMD64 x86 capabilities
  - Specialized engines for specific workloads

The right answer is a combination of these approaches
AMD Opteron™ Processor Directions

2007
- Quad-Core
- On-Chip L3 Cache
- DDR2 Platform Compatible
- Memory RAS
- Enhanced AMD-V

2008
- Large L3 Cache

2009
- Enhanced Direct Connect
  - HyperTransport 3
  - 4 HT links
- Manageability Port
- RAS Enhancements
- Next Generation Core

FOCUS: Performance/Watt/$

GOAL: System Balance
- Scale CPU performance
- Scale I/O bandwidth
- Scale memory capacity
- Scale memory bandwidth
Mid 2007: AMD Opteron™ Processor - “Barcelona”

- **Performance**
  - Quad-Core
    - Enhanced CPU IPC
    - 4x 512K L2 cache
    - 2MB L3 Cache
  - Direct Connect Architecture
    - HyperTransport™ Technology 1.0, 8 GB/s
  - Floating Point
    - 128-bit FPU per core
    - 4 FLOPS/clk peak per core
  - Memory
    - 1GB Page Support
    - DDR-2 up to 667/800* MHz
  - Enhanced Virtualization
    - Nested Page Tables

- **Scalability**
  - 48-bit Physical Addressing

- **Compatibility**
  - Same Socket, Pkg. and Platforms
  - Option for Board Enhancements

*Available 1H08
Investment Protection: Stable Platform Progression

*Long-term success for partners and end-customers*

Stable platforms deliver better long-term value and logical transitions for partners and customers.
Direct Connect Architecture
“Torrenza” Program

Gaming Physics Accelerator

XML Accelerator

Partner Optimized Silicon

PCI-E Bridge

FLOPs Accelerator

I/O Hub

USB

PCI

8 GB/S

8 GB/S

8 GB/S

8 GB/S

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HyperTransport™ 3.0

Same Features as HyperTransport 2.0 Plus:
- 1.8 GHz, 2.0 GHz, 2.4 GHz and 2.6 GHz Clock Support
  - 41.6 GB/s Aggregate Bandwidth
  - 20.8 GB/s (166.4 Gb/s) per Link
- DC Operating Mode Enhancements
- AC Operating Mode (Optional)
  - Supports Applications Requiring Greater Signal Interconnect Distance: Cables, Backplanes, Larger Physical Systems, Chassis-To-Chassis Connections
- DC/AC Auto-Configuration
- Link-Splitting/Un-Ganging Mode (Optional)
  - Auto-configuration of Bi-Mode 2x8 or 1x16 Links
- Hot Plugging
  - Backplanes Applications
- Power Management Enhancements (Optional)
  - Support Dynamic Link Frequency and Width
- 100% Backward Compatibility
  - Auto-Configuration at Boot-Up with Minimum Spec Common Denominator Selection

Double speed
Doubling Today’s State-of-the-Art Performance (HT2.0 with 1.4 GHz Clock and 16-Bit Wide Links) With No Increase in System Design Complexity and Real Estate Penalty/Cost

Flexibility
Allows System Vendors to Connect the Same Device in DC Mode for Short Runs and AC Mode for Long Runs

Lower latency
Auto-Configuration of Bi-Mode 2x8 or 1x16 Link
More HyperTransport Ports Useful in Topologies Such As Symmetric Multi-Processing (SMP) Required by Vendors Interested in Dual-Mode
Up to Four 16-bit HyperTransport™ links or Eight 8-bit Links

Increased number of higher bandwidth links for optimum multi-processor application performance

Fully connected 4-socket node

Fully connected 8-socket node with direct connect between memory controllers

Faster links and few hops = better memory latency
Stream Computing – Proof of Concept Projects

- Traditional HPC
  - Seismic processing
  - Financial analysis
  - Genetic research
- Folding @Home: 40x CPU
- Embedded OEM
  - Medical imaging
  - Signal processing
AMD Stream Processors

- FireStream 580 delivered excellent results
  - 120GFLOPS matrix multiply (180GFLOPS on R600)
  - 50GFLOPS FFT
- R600 is being tested in a variety of applications
- Future streams boards for deployment will emphasize features for computation:
  - IEEE 754 enhancements
  - Double-precision floating point beginning in early 2008
  - Memory export beginning in early 2008
  - Investigating error detection/correction, other architectural enhancements
Stream Computing Development
Open Systems Approach

Brook+
- High-level language, C-like compiler for the GPU
- Based on Brook from Stanford; AMD enhancements to Brook API will be open-sourced

Libraries
- AMD’s math libraries ACML and APL provide GPU-accelerated math functions; COBRA video library accelerates video transcode

CAL – Compute Abstraction Layer
- Provides low-level access to GPU architecture
- Published instruction set architecture (ISA) and intermediate language (IL) allow developers to write in Brook+ or other HLL; then tune performance at low level
- Forward compatibility with R600 and future GPUs
- Implements new features: DX10, DP-FP

3rd Party Tools
- Tools and libraries from RapidMind, Havok, universities, and other partners
Streams Computing
Software Development Tools

Stream Applications

Compilers
- Brook

Libraries
- ACML
- Cobra

3rd Party Tools
- Rapidmind
- Havok
- Microsoft FXC (HLSL)

AMD Runtime

Compute Abstraction Layer (CAL)

Close-to-Metal (CTM)

AMD Stream Processors

Graphics API
- Direct X
- OpenGL

CAL Graphics Binding

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Stream Computing Roadmap

Q4'07

Hardware
- Developer Kit
- New FireStream boards with DP-FP
- MXM: for embedded applications
- OEM Systems

Q1'08

Q2'08

Q3'08

Q4'08

Tools
- SDK Beta (October)
  - CAL
  - Brook
  - IL, ISA specs
  - Programming guide
  - Installation guide

- SDK 1.0 release
  - Brook+
  - CAL
  - ISA, IL specs
  - Programming guide
  - Installation guide
  - ACML, APL
  - Linux
  - Multi-GPU
  - XP
  - XP Server
  - RapidMind

- SDK 2.0 release
  - Additional library routines
  - Enhancements

OEM Systems

Next gen. FireStream boards

2007 Worldwide High Performance Computing
AMD in HPC

History

1999 AMD at Microprocessor Forum announces X86-64, Multi-core and Direct Connect Architecture based on HyperTransport™

2001 AMD enters the HPC markets with its 7th generation CPU AthlonMP™

2002 AMD starts development of eco-system on applications, tools, compilers and mathematical libraries

2003 AMD Opteron™ is delivered on promise. It is the first X86-64 CPU in the market and its DCA offers low latency and high bandwidth

2005 AMD Opteron™ Dual Core is the first X86 multi-core. It is power and pin compatible with single core and DCA allows high scalability and efficiency

2006 All T1 OEMs have AMD-based products in their HPC products portfolio. AMD acquires ATI and announces future architectures based on CPUs, GPUs, Accelerators and ‘Fusion’ on die of these elements

2007 AMD launches its Opteron™ native Quad Core. It is pin and power compatible with DC and integrates strong enhancements for the HPC market
Continuum of Solutions

Accelerated Computing

"Torrenza"

"Fusion"

Package level integration (MCM)

Silicon level integration

Accelerated Processors

Fusion – AMD’s code name for: Accelerated Processors (integrated acceleration)

Torrenza – AMD’s code name for: slot or socket based acceleration

Stream – Specific example of a GPGPU accelerator under Torrenza

Socket compatible accelerator

"Stream" general purpose GPU

"Stream" general purpose GPU

Slot or Socket Acceleration

2007 Worldwide High Performance Computing
AMD's Flexible, Modular Design Approach for Increased Agility

Modular approach accelerates time to market, increased flexibility and agility
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  - HPC WW
  - AMD HPC WW
WW HPC Markets and Segments

IDC HPC Breakfast Briefing June 27, 2007

All Servers $52B
- Business Servers $42B
- HPC Servers $10B +9%
  - Supercomputers (Over $500K) $2.4B
  - Divisional ($250K - $500K) $1.6B
  - Departmental ($250K - $50K) $3.6B
  - Workgroup (under $50K) $2.5B
- Government/Defense
- Industry/Private Sector
- Academic/University

HPC Servers $10B +9%

2007 Worldwide High Performance Computing
Platforms in Market Today

2003 vs. 2007

IBM eServer 325

1st Generation AMD Opteron™

XT4
XT3™
X3455
X2100
U20 & U40 WS
Blade X6220
Blade X8420
X4500
X4600
X2200
X4200/4100
SC 1435
PowerEdge 2970
PowerEdge 6950
DL585
DL385
DL365
DL145
BL465c
BL685c
xw9400
E-9422R
E-9522R
E-9722R
E-9222T
XT3™
XT4
G5450

E-9222T

X630 S2

AMD Validated Solutions

BladeFrame ES and EX

EMBARGOED UNTIL SEPTEMBER 10

2003 vs. IBM eServe

1st Generation AMD Opteron™

2007

AMD Opteron™

47

2970

Validated Solutions

Blades X6220
Blades X8420

SC 1435

PowerEdge 6950

DL585
DL385
DL365
DL145
BL465c
BL685c
xw9400

E-9422R
E-9522R
E-9722R
E-9222T

XT3™
XT4

G5450

EMBARGOED UNTIL SEPTEMBER 10
AMD in HPC
New Organization – Divisions involved

HPC CTO Office
(Rich Oehler)

HPC Business Development
(Francesco Torricelli)

HPC Server/WS Division
(David Rich)

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(Rich Oehler)

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(Francesco Torricelli)

HPC Server/WS Division
(David Rich)

TORRENZA
(Doug O’Fraherty/Jay Owen)

ATI Stream Processor
(Patti Harrell)

Global Solution Team
(Alexandra Bialek)

Tools Division
(Rajeev Gulati)

HPC Performance Division
(Bill Brantley)

HPC Interconnect - ISV Division
(Scot Schultz)

SW Division
(Kevin Wagner)

2007 Worldwide High Performance Computing
AMD in HPC
Locations

- Sunnyvale, California
  - ISV Division (Kevin Wagner)
  - HPC Interconnect (Scot Schultz)
  - Developer Center (Matt Wise)

- Austin, Texas
  - Performance Division (Mike Goddard)

- Frimley, UK
  - NAG

- Pisa, Italy

- Bangalore, India

- Tokyo, Japan
  - TOKYO Lab

PGI, Portland
- Tools Division (Rajeev Gulati)
# AMD in HPC

**Software Development Tools**

http://developer.amd.com/downloads.jsp

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The AMD CodeAnalyst™ Performance Analyzer is a suite of powerful tools that analyze software performance on AMD microprocessors. These tools are designed to support Windows, Linux, and Macintosh operating systems, and can be used to optimize software performance on AMD processors. The tools include a performance profiler, a performance analyzer, and a performance monitor. The profiler allows you to analyze the performance of your code, while the analyzer provides detailed performance metrics. The monitor allows you to monitor the performance of your system in real-time.

## AMD CodeAnalyst Performance Analyzer

- Learn more about AMD's suite of tools for graphics production and development. Analyze and optimize visual applications and models for maximum performance.

## AMD Graphics Tools (formerly ATI Tools)

The AMD Graphics Tools (formerly ATI Tools) are a suite of tools designed to help developers optimize and test their graphics applications. They include tools for profiling, debugging, and optimizing graphics applications. The tools are available for Windows, Linux, and Macintosh operating systems.

## AMD Core Math Library (ACML)

The AMD Core Math Library (ACML) is a collection of numeric libraries that provide high-performance mathematical and statistical routines for scientific and engineering applications. The libraries are available for Windows, Linux, and Macintosh operating systems.

## AMD Performance Library (APL)

The AMD Performance Library (APL) is a collection of libraries that provide high-performance numerical routines for scientific and engineering applications. The libraries are available for Windows, Linux, and Macintosh operating systems.

## AMD "SIMFIRE": Interoperability Test Tools for DMTF DASH

The AMD "SIMFIRE" test tool suite is designed to test the DASH environment in a variety of conditions. The tool suite includes a set of benchmarks that can be used to evaluate the performance of different systems and configurations. The benchmarks include tests for memory access, disk I/O, network performance, and more.

## AMD GCC RPMS

The AMD GCC RPMS are a collection of RPM packages that provide the AMD GCC compiler. The packages are available for various Linux distributions, including Red Hat, SUSE, and Fedora.

## AMD SimNow™ Simulator

The AMD SimNow™ Simulator is a software tool that allows developers to simulate the performance of their applications on AMD processors. The simulator allows you to test your applications in a variety of conditions, including different memory architectures, operating systems, and processors.

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## AMD Software Development Tools

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## AMD Software Development Tools

The AMD Software Development Tools (SDDT) are a suite of tools designed to help developers optimize and test their applications. They include tools for profiling, debugging, and optimizing applications. The tools are available for Windows, Linux, and Macintosh operating systems.

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## AMD Software Development Tools

The AMD Software Development Tools (SDDT) are a suite of tools designed to help developers optimize and test their applications. They include tools for profiling, debugging, and optimizing applications. The tools are available for Windows, Linux, and Macintosh operating systems.
AMD in HPC
HPC Website
www.amd.com/hpc