Lecture 2
A General Discussion on Parallelism

John Cavazos
Dept of Computer & Information Sciences
University of Delaware

www.cis.udel.edu/~cavazos/cisc879
Lecture 2: Overview

- Flynn’s Taxonomy of Architectures
- Types of Parallelism
- Parallel Programming Models
- Commercial Multicore Architectures
Flynn’s Taxonomy of Arch.

- SISD - Single Instruction/Single Data
- SIMD - Single Instruction/Multiple Data
- MISD - Multiple Instruction/Single Data
- MIMD - Multiple Instruction/Multiple Data
Single Instruction/Single Data

The typical machine you’re used to (before multicores).


CISC 879 : Advanced Parallel Programming
Processors that execute same instruction on multiple pieces of data.

CISC 879 : Advanced Parallel Programming
Single Instruction/Multiple Data

- Each core executes same instruction simultaneously
- Vector-style of programming
- Natural for graphics and scientific computing
- Good choice for massively multicore
SIMD very often requires compiler intervention.

Slide Source: ars technica, Peakstream article

CISC 879 : Advanced Parallel Programming
Multiple Instruction/Single Data

Only Theoretical Machine. None ever implemented.


CISC 879 : Advanced Parallel Programming
Many mainstream multicore processors fall into this category.
Multiple Instruction/Multiple Data

- Each core works independently, simultaneously executing different instructions on different data.
- Unique upper levels of cache and may have lower level of shared cache.
- Cores can have SIMD-extensions.
- Programmed with a variety of models (OpenMP, MPI, pthreads, etc.)
Lecture 2: Overview

- Flynn’s Taxonomy of Architecture
- Types of Parallelism
- Parallel Programming Models
- Commercial Multicore Architectures
Types of Parallelism

Instructions:

Pipelining

Data-Level Parallelism (DLP)

Thread-Level Parallelism (TLP)

Instruction-Level Parallelism (ILP)

CISC 879 : Advanced Parallel Programming

Slide Source: S. Amarasinghe, MIT 6189 IAP 2007
Pipelining

IF: Instruction fetch
EX: Execution
ID: Instruction decode
WB: Write back

Cycles

<table>
<thead>
<tr>
<th>Instruction #</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction i</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction i+1</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction i+2</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction i+3</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction i+4</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Corresponds to SISD architecture.

Slide Source: S. Amarasinghe, MIT 6189 IAP 2007
Instruction-Level Parallelism

Dual instruction issue superscalar model. Again, corresponds to SISD architecture.

Slide Source: S. Amarasinghe, MIT 6189 IAP 2007
Data-Level Parallelism

Data Stream or Array Elements

What architecture model from Flynn’s Taxonomy does this correspond to?

Slide Source: Arch. of a Real-time Ray-Tracer, Intel
Data-Level Parallelism

Data Stream or Array Elements

Corresponds to SIMD architecture.

Slide Source: Arch. of a Real-time Ray-Tracer, Intel
One operation (e.g., +) produces multiple results. \( X \), \( Y \), and result are arrays.
Program partitioned into four threads.

Four threads each executed on separate cores.

What architecture from Flynn’s Taxonomy does this correspond to?

Multicore with 6 cores.

CISC 879 : Advanced Parallel Programming

Slide Source: SciDAC Review, Threadstorm pic.
Thread-Level Parallelism

Program partitioned into four threads.

Four threads each executed on separate cores.

Corresponds to MIMD architecture.

Multicore with 6 cores.

CISC 879 : Advanced Parallel Programming
Lecture 2: Overview

- Flynn’s Taxonomy of Architecture
- Types of Parallelism
- Parallel Programming Models
- Commercial Multicore Architectures
Multicore Programming Models

- Message Passing Interface (MPI)
- OpenMP
- Threads
  - Pthreads
  - Cell threads
- Parallel Libraries
  - Intel’s Thread Building Blocks (TBB)
  - Microsoft’s Task Parallel Library
  - SWARM (GTech)
  - Charm++ (UIUC)
  - STAPL (Texas A&M)
**GPU Programming Models**

- **CUDA (Nvidia)**
  - C/C++ extensions
- **Brook+ (AMD/ATI)**
  - AMD-enhanced implementation of Brook
- **Brook (Stanford)**
  - Language extensions
- **RapidMind platform**
  - Library and language extensions
  - Works on multicores
  - Commercialization of Sh (Waterloo)
Lecture 2: Overview

- Flynn’s Taxonomy of Architecture
- Types of Parallelism
- Parallel Programming Models
- Commercial Multicore Architectures
Generalized Multicore

L1 Cache - L1 Cache - L1 Cache - L1 Cache

L2 Cache - L2 Cache

L3 Cache


CISC 879: Advanced Parallel Programming
Cell B.E. Architecture


CISC 879 : Advanced Parallel Programming
## Commercial Multicores

<table>
<thead>
<tr>
<th>Name</th>
<th>Clovertwn</th>
<th>Opteron</th>
<th>Cell</th>
<th>Niagara 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips*Cores</td>
<td>2*4 = 8</td>
<td>2*2 = 4</td>
<td>1*8 = 8</td>
<td>1*8 = 8</td>
</tr>
<tr>
<td>Architecture</td>
<td>4-/3-issue, SSE3, OOO, caches</td>
<td>2-VLIW, SIMD, RAM</td>
<td>1-issue, MT, cache</td>
<td></td>
</tr>
<tr>
<td>Clock Rate</td>
<td>2.3 GHz</td>
<td>2.2 GHz</td>
<td>3.2 GHz</td>
<td>1.4 GHz</td>
</tr>
<tr>
<td>Peak MemBW</td>
<td>21 GB/s</td>
<td>21 GB/s</td>
<td>26 GB/s</td>
<td>41 GB/s</td>
</tr>
<tr>
<td>Peak GFLOPS</td>
<td>74.6 GF</td>
<td>17.6 GF</td>
<td>14.6 GF</td>
<td>11.2 GF</td>
</tr>
</tbody>
</table>

Slide Source: Dave Patterson, Manycore and Multicore Computing Workshop, 2007