

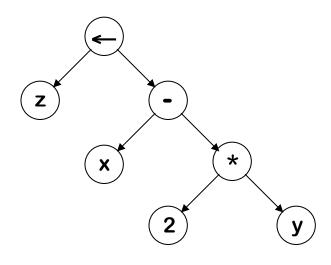


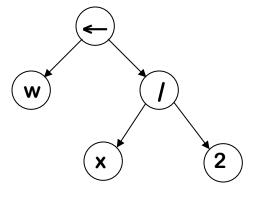
# Intermediate Representations Part II

Directed Acyclic Graph



A directed acyclic graph (DAG) is an AST with a unique node for each value





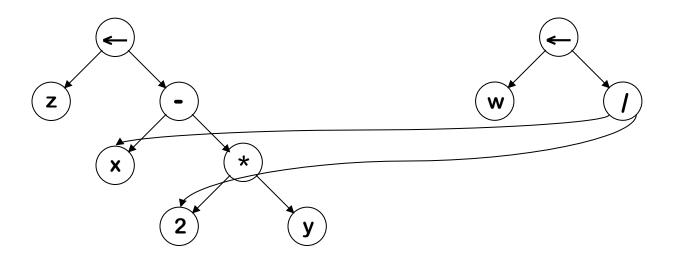
z ← x - 2

w ← x / 2

Directed Acyclic Graph



A directed acyclic graph (DAG) is an AST with a unique node for each value



z ← x - 2

w ← x / 2

Stack Machine Code



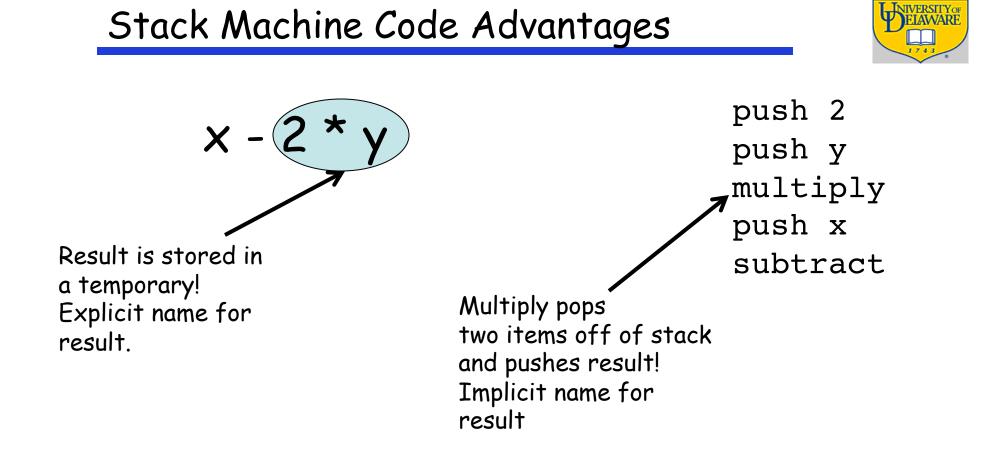
Originally used for stack-based computers, now Java

• Example:

push x
push 2
push y
multiply
subtract



- Operations take operands from a stack
- Compact form
- A form of one-address code
- Introduced names are *implicit*, not *explicit*
- Simple to generate and execute code



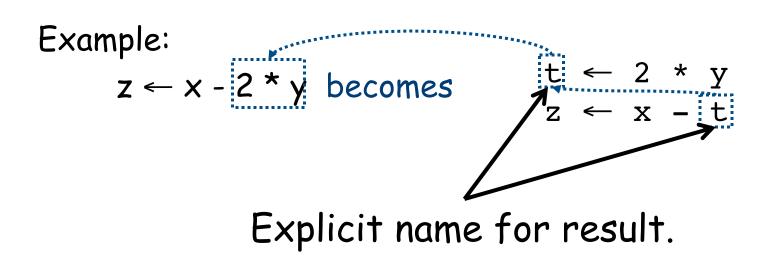


Different representations of three address code

 In general, three address code has statements of the form:

With 1 operator (<u>op</u>) and (at most) 3 names (x, y, & z)





Three Address Code Advantages



- Resembles many real (RISC) machines
- Introduces a new set of names
- Compact form



Naïve representation of three address code

Table of k \* 4 small integers

load	r1,	У	
loadI	r2,	2	
mult	r3,	r2,	r1
load	r4,	X	
sub	r5,	r4,	r3

Dest	ination	l	
		Two oj	perands
	V		
load	1	У	
loadi	2	2	
mult	3	2	1
load	4	x	
sub	5	4	3

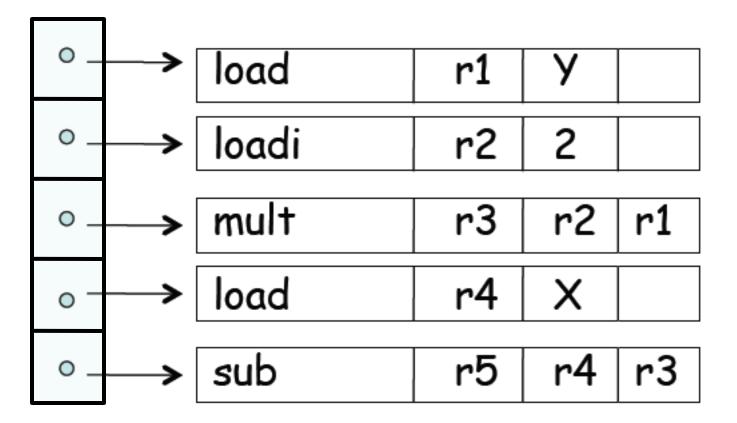
RISC assembly code

Quadruples



Three Address Code: Array of Pointers

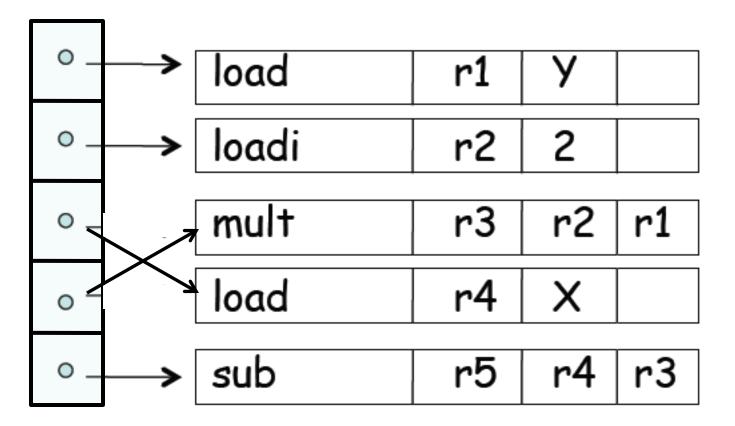
- Index causes level of indirection
- Easy (and cheap) to reorder
- Easy to add (delete) instructions





Three Address Code: Array of Pointers

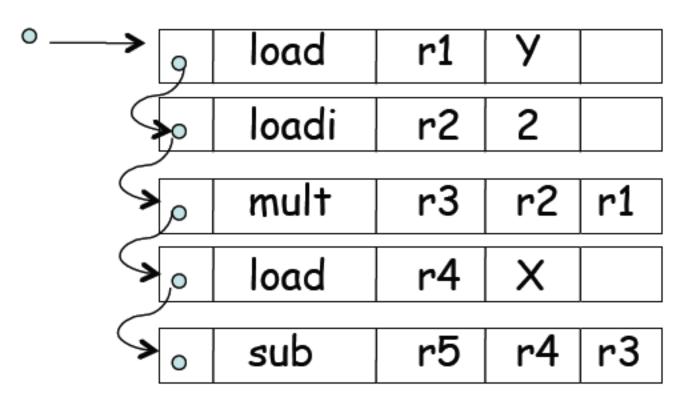
- Index causes level of indirection
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Three Address Code: Array of Pointers



- No additional array of indirection
- Easy (and cheap) to reorder than simple table
- Easy to add (delete) instructions



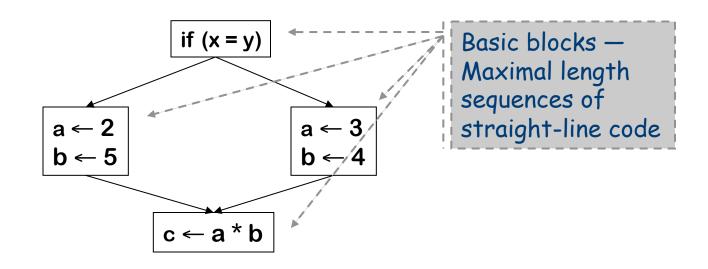
## Control-flow Graph



Models the transfer of control in the procedure

- Nodes in the graph are basic blocks
  - Can be represented with quads or any other linear representation
- Edges in the graph represent control flow

Example





Node: an instruction or sequence of instructions (a basic block)

→ Two instructions i, j in same basic block *iff* execution of i *guarantees* execution of j

- Directed edge: *potential* flow of control
- Distinguished start node Entry
   First instruction in program

# **Identifying Basic Blocks**



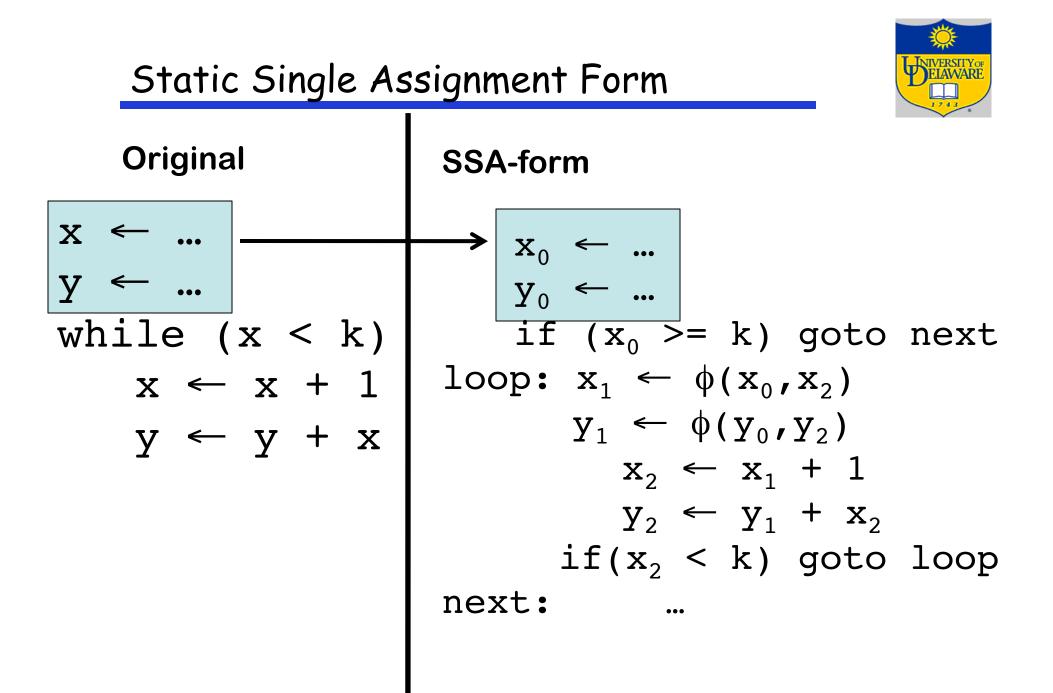
- Input: sequence of instructions instr(i)
- Identify leaders: first instruction of basic block
- Iterate: add subsequent instructions to basic block until we reach another leader

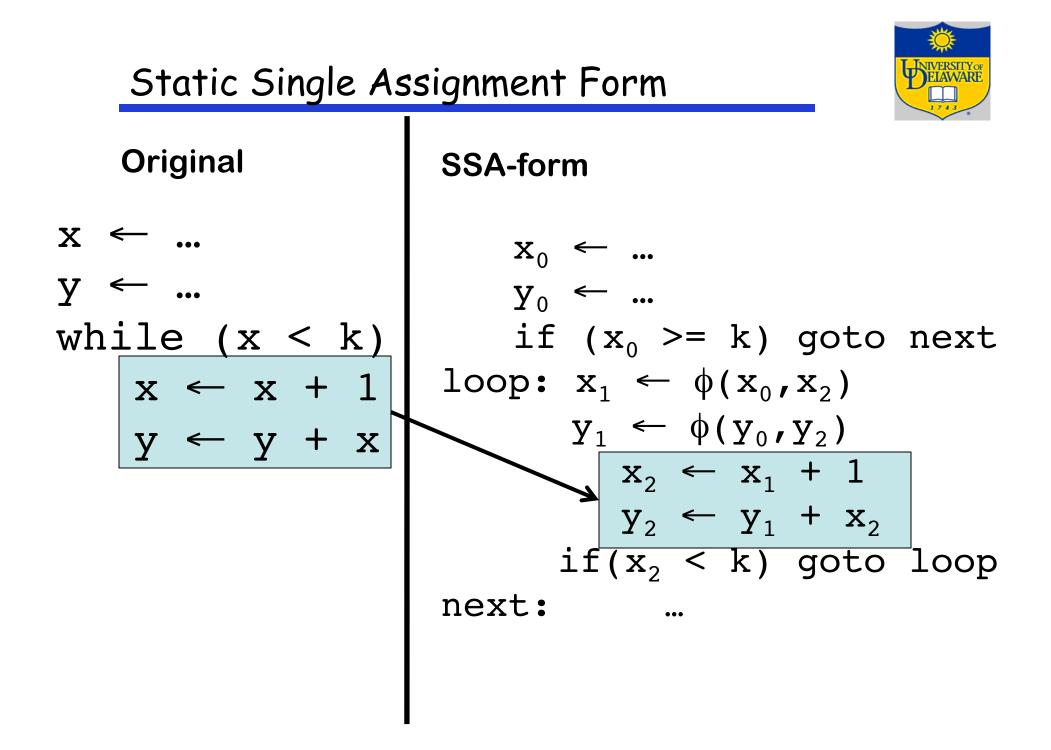


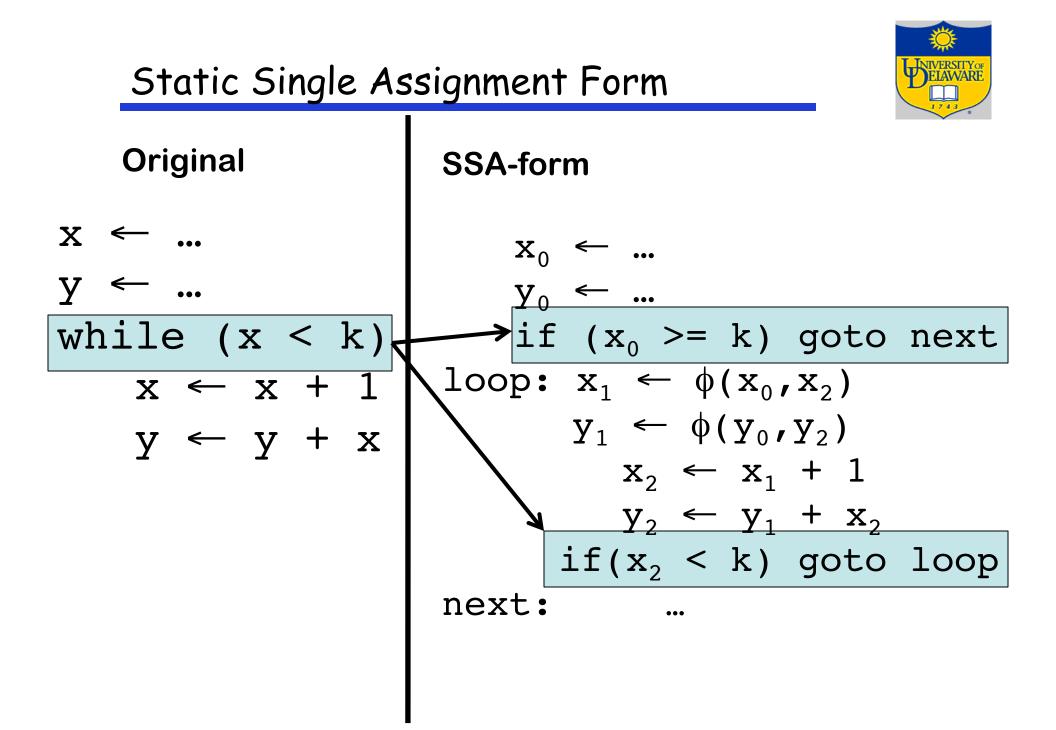
```
leaders = instr(1) // first instruction
```

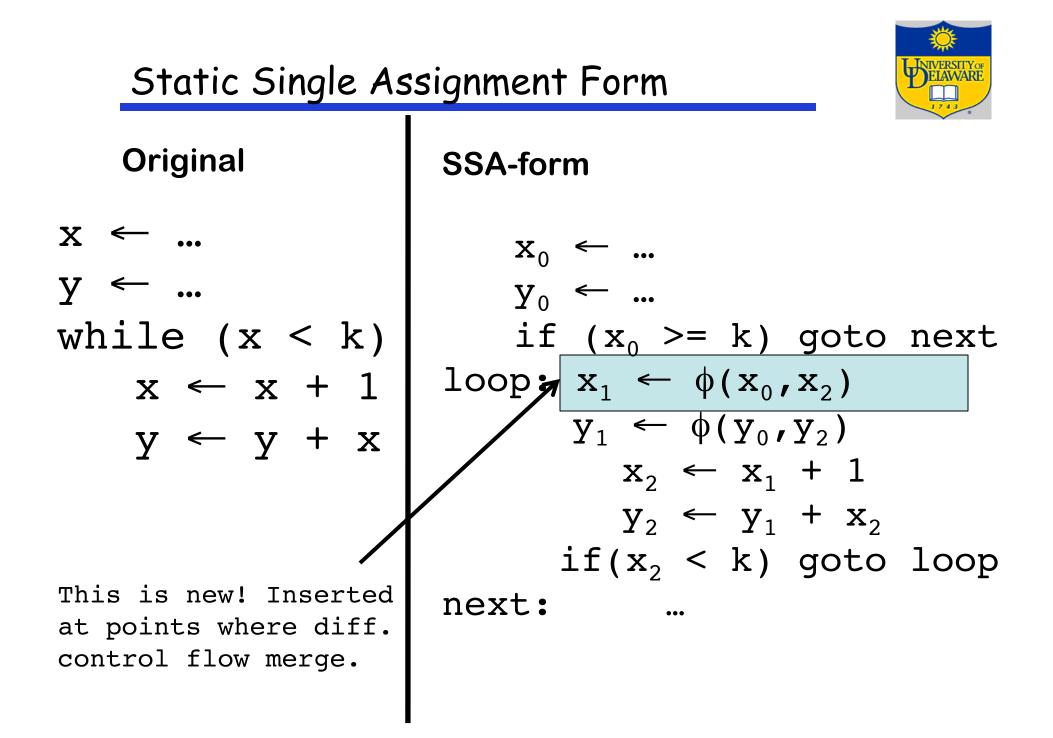
```
worklist = leaders
While worklist not empty
x = first instruction in worklist
worklist = worklist - {x}
block(x) = {x}
for (i = x + 1; i <= |n| && i not in leaders; i++)
block(x) = block(x) ∪ {i}</pre>
```

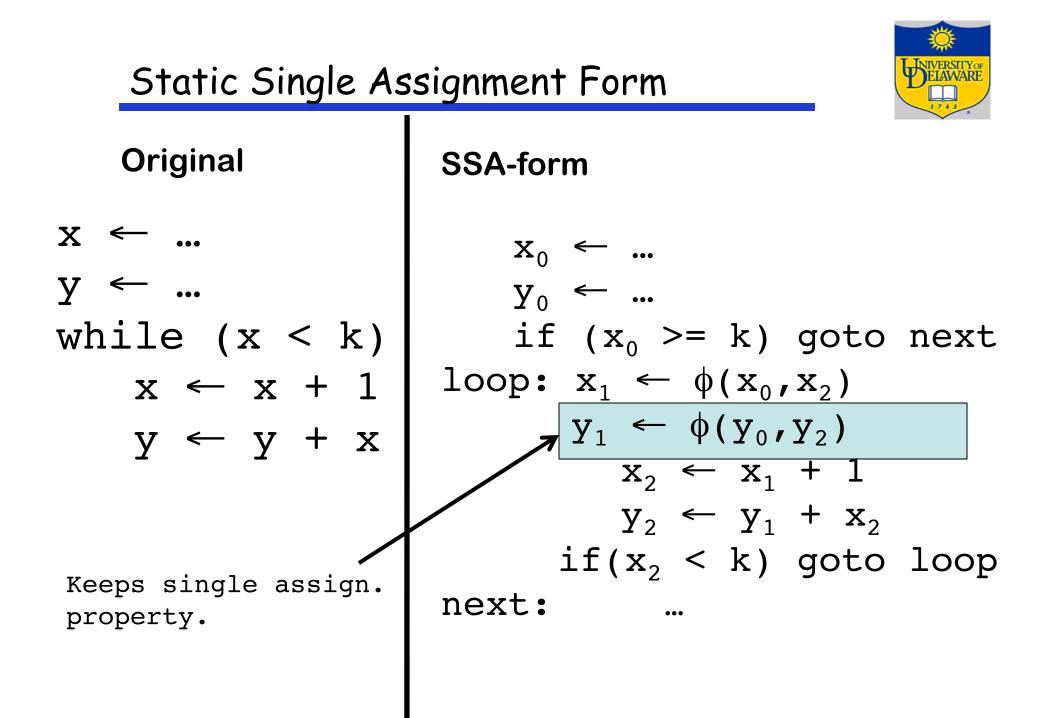
Static Single Assignment Form		
Original	SSA-form	
$x \leftarrow \dots$ $y \leftarrow \dots$ while $(x < k)$ $x \leftarrow x + 1$ $y \leftarrow y + x$	$\begin{array}{rcl} x_{0} \leftarrow & \dots & & \\ y_{0} \leftarrow & \dots & & \\ \text{if } (x_{0} \geq k) \text{ goto next} \\ \text{loop: } x_{1} \leftarrow & \varphi(x_{0}, x_{2}) & & \\ y_{1} \leftarrow & \varphi(y_{0}, y_{2}) & & \\ x_{2} \leftarrow & x_{1} + 1 & & \\ y_{2} \leftarrow & y_{1} + x_{2} & & \\ \text{if}(x_{2} < k) \text{ goto loop} \\ \text{next: } & \dots & \end{array}$	











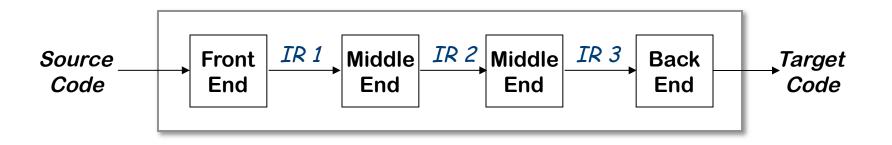
Static Single Assignment Form Advantages



Strengths of SSA-form

- Sharper analysis because values never redefined
- Simplifies and improves optimizations
- (Sometimes) faster algorithms





- Repeatedly lower the level of the intermediate representation
  - → Each intermediate representation is suited towards certain optimizations
- Example: the Open64 compiler
  - → WHIRL intermediate format
    - Consists of 5 different IRs that are progressively more detailed and less abstract

### Memory Models

Two major models

- Register-to-register model
  - $\rightarrow$  Keep all values that can legally be stored in a register in registers
  - $\rightarrow$  Ignore machine limitations on number of registers
  - → Compiler back-end must insert loads and stores
- Memory-to-memory model
  - $\rightarrow$  Keep all values in memory
  - → Only promote values to registers directly before they are used
  - → Compiler back-end can remove loads and stores
- Compilers for RISC machines usually use register-to-register
  - → Reflects programming model
  - $\rightarrow$  Easier to determine when registers are used



The Rest of the Story...



Representing the code is only part of an *IR* 

There are other necessary components

- Symbol table
- Constant table
  - $\rightarrow$  Representation, type
  - → Storage class, offset
- Storage map
  - → Overall storage layout
  - $\rightarrow$  Overlap information
  - $\rightarrow$  Virtual register assignments

#### Symbol Tables

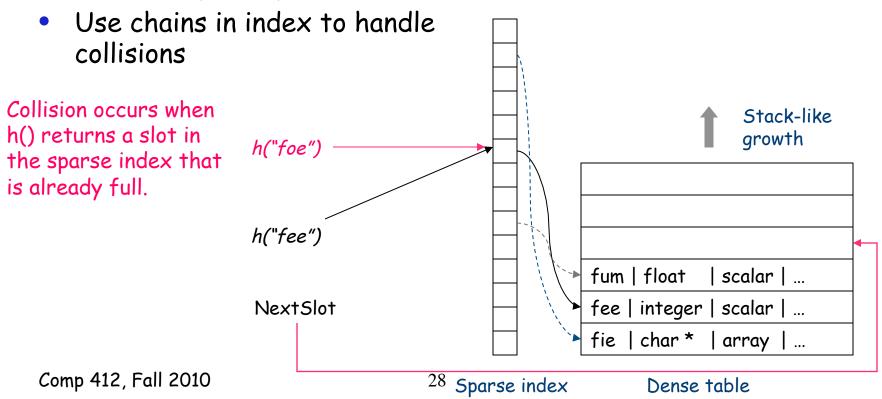


See §B.3 in FaC for

a longer explanation

Classic approach to building a symbol table uses hashing

- Personal preference: a two-table scheme
  - $\rightarrow$  Sparse index to reduce chance of collisions
  - $\rightarrow$  Dense table to hold actual data
    - Easy to expand, to traverse, to read & write from/to files

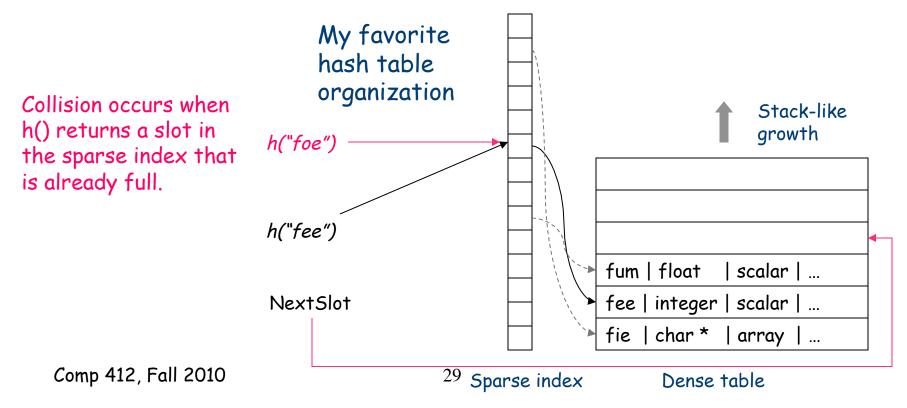


### Hash-less Symbol Tables



Classic approach to building a symbol table uses hashing

- Some concern about worst-case behavior
  - $\rightarrow$  Collisions in the hash function can lead to linear search
  - → Some authors advocate "perfect" hash for keyword lookup
- Automata theory lets us avoid worst-case behavior





One alternative is Paige & Cai's *multiset discrimination* 

- Order the name space offline
- Assign indices to each name
- Replace the names in the input with their encoded indices

Digression on page 241 of EaC

Using DFA techniques, we can build a guaranteed linear-time replacement for the hash function *h* 

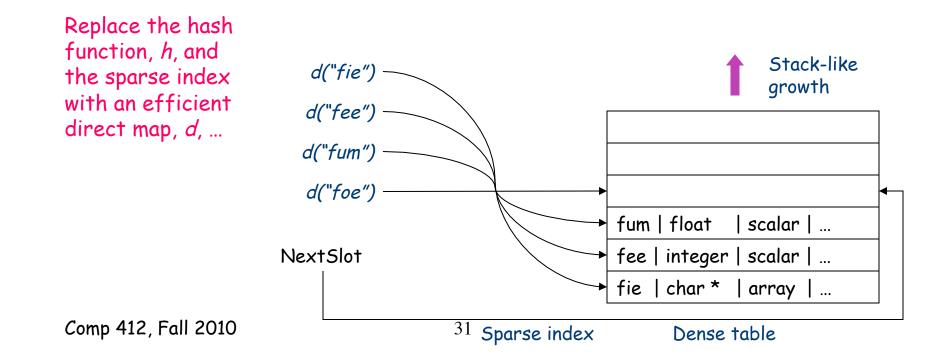
- DFA that results from a list of words is acyclic
  - $\rightarrow$  RE looks like  $r_1 | r_2 | r_3 | ... | r_k$
  - → Could process input twice, once to build DFA, once to use it
- We can do even better

### Hash-less Symbol Tables



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Incremental construction of an acyclic DFA

- To add a word, run it through the DFA
  - $\rightarrow$  At some point, it will face a transition to the error state
  - → At that point, start building states & transitions to recognize it
- Requires a memory access per character in the key
  - $\rightarrow$  If DFA grows too large, memory access costs become excessive
  - $\rightarrow$  For small key sets (e.g., names in a procedure), not a problem
- Optimizations
  - → Last state on each path can be explicit
    - Substantial reduction in memory costs
    - Instantiate when path is lengthened
  - → Trade off granularity against size of state representation
  - → Encode capitalization separately
    - Bit strings tied to final state?