Ge Incorporation in SiC and the Effects on Device Performance

K. J. Roe, M. W. Dashiell, <u>G. Xuan</u>*, E. Ansorge, G. Katulka, N. Sustersic, X. Zhang and
J. Kolodzey
Department of Electrical and Computer Engineering
140 Evans Hall
University of Delaware
Newark, DE 19716, U.S.A.

Abstract

Silicon carbide has been given much attention as a promising material for use in high-voltage and high-power devices. The absence of closely lattice-matched materials precludes the existence of heterostructure devices with good properties. The availability of a lattice-matched heterojunction partner should allow for new SiC-based devices that can exploit the heterojunction band offsets to enhance device properties.

Silicon-carbide:Germanium (SiC:Ge) alloy was formed by ion implantation of Ge into 4H-SiC wafers at 1000 ^{o}C. We have observed the resultant SiC:Ge material to have favorable properties, such as nice crystal structure, interface quality and good electrical characteristics.

Diodes and bipolar transistors have been fabricated using these layers. These devices have been characterized for properties including forward current density and transistor gain. In this paper we report on the effects of Ge incorporation on devices formed using SiC:Ge layers.

SiC:Ge Alloy

The concept of Ge incorporating into SiC is illustrated in Figure 1. The SiC:Ge alloy was fabricated by low-energy ion implantation. Ge^+ ions were implanted at 140KeV and 50KeV into a   4H-SiC wafer heated to 1000 ^{o}C. The wafer was purchased from Cree Inc, <0001>, N-type and ρ=0.059 Ω-cm. This results in a step-like Ge profile starting at the surface and extending 1200 Å into the substrate, as shown in Figure 2. The composition profile was later checked with Rutherford Backscattering Spectrometry (RBS), which verified the presence of Ge in the substrate. HRXRD (High Resolution X-Ray Diffraction) spectra were measured with a Phillip's X'Pert diffractometer equipped with a four-crystal Ge(220) monochromator and Ge channel-cut analyzer on the primary and detector optical arms respectively. Figure 3 displays the (0004) HRXRD spectra from as-implanted SiC:Ge with 0.4% Ge incorporation together with a non-implanted 4H-SiC control sample. The

Pendellösung (thickness) fringes of SiC:Ge in Figure 3 indicate good crystalline quality and a coherent interface [1]. No such fringes have previously been noted in implanted SiC substrates, presumably due to heavy lattice damage [2, 7]. The strained layer thickness (t) can be calculated from the fringe period ($\Delta\Theta$), X-Ray wavelength (λ=1.54 Å) and the Bragg angle (Θ_B) with the equation:

$$t = \frac{\lambda \sin \Theta_B}{\Delta\Theta \sin 2\Theta_B}$$

From the data in Figure 3 the strained layer thickness t is calculated as 140 ± 20 nm, in good agreement with the projected Ge depth profile simulated by SRIM 2000.

Optical properties of the SiC:Ge material were studied using Raman Spectroscopy and UV-Visible spectrometry techniques. Raman Spectroscopy measurements were performed using a green laser system (λ = 532 nm). The presence of the characteristic (796 cm^{-1} and 972 cm^{-1}) peaks in the Ge implanted areas confirmed that the 4H-SiC structure was reconstructed after the high-temperature anneals. UV-visible measurements were performed in transmission mode over the $190 - 1100$ cm^{-1} wavelength region. Analysis of the absorption spectra using the MacFarlane-Roberts equations yielded a decrease in the optical bandgap of 100 meV for a layer with 2.2 atomic % of Ge.

These results suggest that low energy implantation can form SiC:Ge alloy with good crystal and interface quality and lower optical bandgap, thus crediting the potential for fabricating SiC:Ge/SiC heterostructures.

TLM Measurements on SiC:Ge layer

To do the contact studies, TLM (Transfer Length Method) patterns were fabricated on both n-type and p-type SiC:Ge samples together with SiC ones for comparison [5]. Both the p-type and n-type SiC:Ge samples were used with approximately two atomic percent of Ge.

The TLM measurements showed a significant reduction in contact resistivity: from 5.3 x 10^{-4} Ω-cm^2 to 6.0 x 10^{-5} Ω-cm^2 for n-type SiC:Ge; and from 1.2 x 10^{-3} Ω-cm^2 to 8.3 x 10^{-5} Ω-cm^2 for p-type case. And calculations showed a reduction in the effective barrier height by 57 mV and 70 mV, respectively for n-type and p-type SiC:Ge. Table I summarizes the TLM measurement results. These results suggest the potential of Ge containing layers to become an important processing technique to lower the contact resistance with SiC.

SiC:Ge/SiC heterojunction diodes

SiC:Ge/SiC heterojunction diodes and reference SiC p-n junction ones were fabricated using Ti/Au metal as electrical contacts[3].

The current-voltage characteristics on the SiC:Ge/SiC diodes were measured and summarized in Table II. The data was found to fit well to a simple theory of injection over a heterojunction barrier, as shown in Figure 4. A typical current voltage plot of the SiC:Ge heterojunction and SiC homojunction diodes is given in Figure 5. The incorporation of Ge was found to increase the diode current density and decrease the heterojunction ideality factor from 1.88 to 1.48. The greater asymmetry between forward and reverse current (larger rectification ratio) for the SiC:Ge devices suggests the presence of band offsets. Capacitance-voltage measurements show that that the Ge also reduced the measured built-in voltage. This result was found to be consistent with the observed difference in layer contact resistances [5].

SiC/SiC:Ge/SiC p-n-p heterojunction bipolar junction transistors (HBTs)

SiC/SiC:Ge/SiC p-n-p heterojunction and SiC p-n-p homojunction bipolar junction transistors (BJTs) were fabricated by ion implantation and annealing[4]. The collector regions were the bulk of a 4H-SiC p-type (approximately 2×10^{16} cm^{-3}) wafer. The p+-emitter regions were formed by the implantation of Ga. The SiC:Ge base region was formed by the co-implantation of Ge and N. A two-step implant anneal was performed at 1050 ^{o}C for 30 minutes and then 1600 ^{o}C for 30 minutes. Simple mesa transistors were then fabricated with RIE etching.

The electrical properties of the SiC/SiC:Ge/SiC p-n-p heterojunction and SiC p-n-p homojunction bipolar junction transistors are summarized in Table II. The SiC:Ge devices exhibited higher maximum gain (3.02 vs. 2.21) and larger Early voltage (605 V vs. 321 V) than the SiC BJT counterparts. Figure 6 shows the typical HBT and BJT common emitter current gain versus base-emitter voltage from the respective Gummel Plots. In each case, the breakdown voltage (BV_{CEO}) of the devices exceeded 50 V. The existence of heterojunction offsets should be manifested in the gain and early voltage properties of the devices, similar to effects seen in Si/SiGe/Si transistors [8].

For a transistor with a lower bandgap material in the base, an increase in the gain β, by a factor of $\exp(\Delta E_g / k_B T)$ is expected, where ΔE_g is the bandgap reduction. Based on this and the β increase, ΔE_g is calculated to be 8.1 meV. Also, assuming the bandgap of SiC:Ge alloy is linear with Ge percentage between SiC and Ge, together with the predicted 0.34% of average Ge concentration from SRIM simulations, SiC:Ge alloy should have a ΔE_g of 8.6 meV lower than the bandgap of SiC. These two predicted values agree with each other very well.

For a transistor with a gradient in Ge concentration from the base to collector junction (provided here by the Gaussian nature of the Ge-implant profile), there will also be an increase in the Early Voltage, V_A, by a factor of $\exp(\Delta E / k_B T)$, where ΔE is the bandgap reduction at the collector side of the base compared to the emitter side. From SRIM implantation simulations, we expect the predicted base to collector fraction gradient to be

0.70 atomic percent. This gradient should result in an ΔE of 17.8 meV. From our typical measured Early voltage values, we calculated an ΔE of 16.4 meV, which once again exhibits excellent agreement. These two measurements again indicate heterostructure device behavior.

Conclusion

In conclusion, we have fabricated and characterized SiC:Ge alloy layers. The presence of Ge has proven to lower electrical contact resistances to devices up to a factor of 10. And we fabricated and demonstrated SiC-based heterostructure devices based on these layers. Heterostructure diodes with varying current density and rectification ratio were observed. We have made the first SiC-based HBT devices, and shown that the presence of Ge in the base increases the gain and the Early voltage by as much as 33% over a homojunction BJT fabricated without Ge but otherwise with an identical process. A common-emitter current gain for the HBT of greater than 3 has been achieved. These results show that SiC:Ge is a promising material for a range of SiC-based heterostructure devices.

Acknowledgements

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Table I. Summary of the TLM measurements of SiC:Ge alloy compared with SiC.

Material Type	Contact Resistance R_c (Ohms)	Transfer Length L_t (microns)	Contact Resistivity (Ohms-cm^2)	Barrier Height Reduction (mV)
n-SiC:Ge	35.3	1.71	6.0×10^{-5}	57
n-SiC	196.2	2.70	5.3×10^{-4}	--
p-SiC:Ge	29.7	2.80	8.3×10^{-5}	70
p-SiC	551.8	2.18	1.2×10^{-3}	--

Table II. Summary of the electrical properties of SiC:Ge and SiC diodes, where η is the effective heterojunction ideality factor. The SiC:Ge diodes have a larger current density and rectification ratio, as expected with a heterojunction band offset.

Diode Material	Rectification Ratio (4V)	η	Current Density (@5V) [mA/cm^2]	Specific Contact Resistance [Ω-cm^2]
SiC:Ge	2.79	1.48	650	1×10^{-3}
SiC	1.60	1.88	400	4×10^{-3}

Table III. Summary of the electrical properties of SiC/SiC:Ge/SiC HBT and SiC BJT devices. The calculated average band offset and total band gradient data calculated from the measured device properties are indicated.

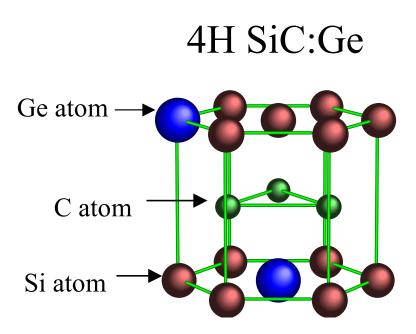| Sample	Common Base Current Gain (α)	Maximum Measured DC gain (β)	Calculated Band offset, ΔE_g [meV]	Early Voltage [V]	Calculated Base Bandgap Gradient [meV]
SiC:Ge HBT	0.850	3.02	8	605	16.4
SiC BJT	0.812	2.21	0	321	0

4H SiC:Ge

Figure 1. Concept of SiC lattice with substitutional Ge atoms, forming a SiC:Ge alloy solid solution.
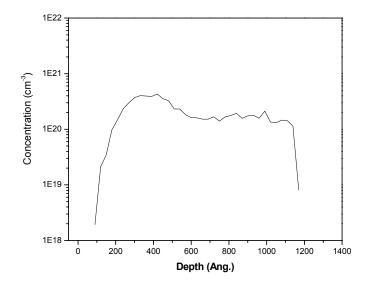

Figure 2. Implanted Ge projected profile simulated by SRIM 2000.
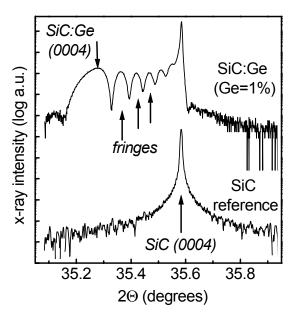
Figure 3. (0004) HRXRD spectra from as-implanted SiC:Ge with 0.4% Ge incorporation together with non-implanted 4H-SiC samples as a reference.
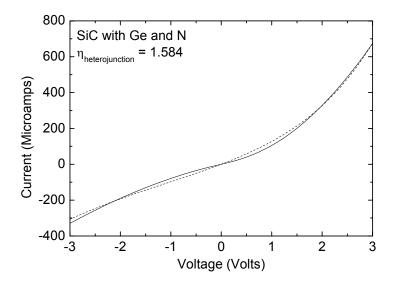

Figure 4. Measured Current-voltage data of a typical SiC:Ge p-n diode (solid line). The dashed curve is a fit of the data with the heterojunction current model that takes into account the heterostructure band offsets as described in the text.
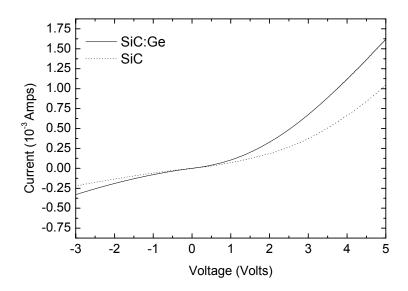
Figure 5. Measured Current-voltage plot of SiC:Ge and SiC diodes. Note the large increase in current density with the presence of Ge.
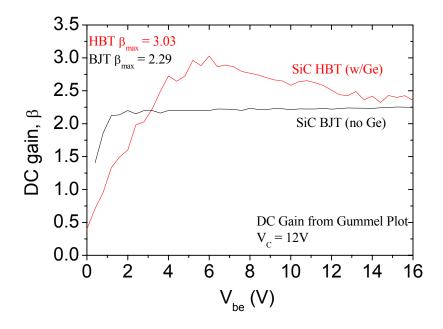

Figure 6. DC current gain, β, versus base-emitter voltage for the SiC:Ge HBT and SiC BJT. Note the larger gain with Ge as expected for a HBT with a heterojunction offset in the base region.