Silicon carbide and silicon carbide:germanium heterostructure bipolar transistors

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In this letter, we report on heterostructure bipolar transistors (HBTs) based on silicon carbide (SiC) and a silicon carbide:germanium (SiC:Ge) alloy. The SiC:Ge base alloy was formed by the ion implantation of Ge into *p*-type 4H–SiC and subsequent annealing. HBT mesa structures were fabricated using a reactive ion etching process. The incorporation of Ge was found to increase the gain and the Early voltage of the devices. A common-emitter current gain (β) of greater than 3 was measured for the SiC:Ge HBTs. Homojunction SiC transistors were fabricated as a reference using the same process (except no Ge in the base region) and exhibited a β of 2.2. The transistors exhibited high breakdown voltages (>50 V without passivation), that typify SiC-based devices. These results indicate that SiC:Ge is a promising material for use in SiC-based heterostructure devices. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1358851]

Silicon carbide has garnered considerable attention as a promising material for use in high-voltage and high-power devices. There are many applications where the superior power handling, mechanical strength, hardness, and thermal conductivity of SiC would give an advantage over Si or GaAs technologies. Clearly, the ability to form heterojunctions gives any material system an advantage. 4H–SiC, with its high band gap (3.2 eV), could function well in a wide-band-gap heterostructure if a suitable second material with a higher or lower band gap were available. Gallium nitride/silicon carbide (GaN/SiC) heterojunction bipolar transistors (HBTs) have recently been reported, but the results could not be easily reproduced due to parasitic defect levels and the inherent difficulty in growing GaN on SiC.[1] Recently, we reported on a SiC:Ge alloy, formed by the implantation of Ge into SiC.[2,3] The data suggest that the incorporation of Ge into a SiC:Ge alloy lowers the band gap by as much as 100 meV. The decrease in band gap was determined by the change in barrier height observed from current–voltage and UV–visible spectroscopy measurements. The possibility of lowering the band gap of 4H–SiC with Ge incorporation makes SiC:Ge attractive for the base region to form SiC HBTs.

The SiC/SiC:Ge/SiC *p–n–p* heterojunction and SiC *p–n–p* homojunction bipolar junction transistors (BJTs) were created by ion implantation and annealing. The collector regions were the bulk of a 4H–SiC *p*-type (approximately $2\times10^{16}\,\mathrm{cm}^{-3}$) wafer. The p^+-emitter regions were formed by the implantation of Ga, which was chosen for its shallow implantation depth at a given energy compared to a lighter atom. The SiC:Ge base region was formed by the coimplantation of Ge as an alloy component and N as the *n*-type dopant. See Table I for a list of implantation conditions. The dopant profiles were identical for both the SiC and the SiC:Ge devices. All implantation steps were performed with no intentional substrate heating. Table II contains the simulated values of implant depth and straggle, and corresponding doping level, as modeled with the implantation simulation program SRIM.[4] The simulated implant distribution versus depth is plotted in Fig. 1. Ge incorporation in the base was confirmed by x-ray diffraction (XRD) measurements, which exhibited a shift in the SiC diffraction peaks due to lattice expansion arising from the larger Ge atoms. Rutherford backscattering spectrometry (RBS) measurements confirmed the concentration and depth of the Ge implant. The reconstruction of the SiC crystal structure after implant annealing was confirmed by the reappearance of SiC phonon modes using Raman spectroscopy measurements.

An implant anneal was performed at 1050 °C for 30 min in a nitrogen ambient. We had observed this to be a sufficient temperature for SiC recrystallization from Raman spectros-

TABLE I. Implant conditions of the SiC/SiC:Ge/SiC *p–n–p* heterojunction and SiC *p–n–p* homojunction transistor samples.

Sample	Region	Implant species	Ion type	Dose (cm^{-2})	Energy (keV)
SiC:Ge HBT	Emitter	Ga	*p* dopant	2.75×10^{14}	225
	Base	N	*n* dopant	1.45×10^{12}	200
	Base	Ge	Alloy	1.00×10^{16}	750
SiC BJT	Emitter	Ga	*p* dopant	2.75×10^{14}	225
	Base	N	*n* dopant	1.45×10^{12}	200

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TABLE II. SRIM simulation of the implant conditions of the SiC/SiC:Ge/SiC $p-n-p$ heterojunction and SiC $p-n-p$ homojunction transistor samples. The Ge concentration of 3.26×10^{20} cm^{-3} corresponds to 0.34 at. %.

Sample	Region:ion	Implant range (Å)	Straggle (Å)	Concentration (cm^{-3})
SiC:Ge HBT	Emitter: Ga	964	220	5.7×10^{19}
	Base: N	2966	579	1.0×10^{17}
	Base: Ge	3054	529	3.26×10^{20}
SiC BJT	Emitter: Ga	964	220	5.7×10^{19}
	Base: N	2966	579	1.0×10^{17}

copy measurements. The implant annealing of SiC for dopant activation, however, is performed at significantly higher temperatures, and a second implant anneal was performed on the devices after the metal contacts were removed. The second anneal was performed at 1600 °C for 30 min in a chemical-vapor-deposition reactor using silane to provide adequate partial pressure of Si to suppress selective outdiffusion of Si from the 4H–SiC surface.[5] After the second implant anneal, the devices were remetallized using an identical process, which is described next. The devices were fully characterized before and after the second implant anneal as described in the next section. The devices showed improvement (50% increase in the gain, β) after the higher-temperature anneal, which we attributed to greater dopant activation and increased material quality.

HBT structures of several geometries were fabricated by patterning and reactive ion etching (RIE). For the data reported in this letter, simple mesa HBTs were created for ease of fabrication and probing (shown in the inset of Fig. 2). Etching was performed in a Plasmatherm 790 RIE system using SF_6:He as the process gases. See Table III for the RIE etch parameters. The emitter, base, and collector contact regions exposed by etching were 80 μm by 80 μm square mesas, with recessed 50 μm square metal contact pads for probing. Thick photoresist (NR7-6000PY) and Ni metal layers were used as etch masks. Etch parameters were optimized on *p*-type trial SiC samples to minimize surface roughness and sample heating. The etch duration was kept to a minimum because the photoresist could be significantly damaged during extended RIE processing. The etch rates of SiC:Ge were found to be about 5% faster compared to SiC under the same conditions. The resultant surface morphology was found to be comparable to *p*-type SiC.

Thermally evaporated nickel was used as the contact to

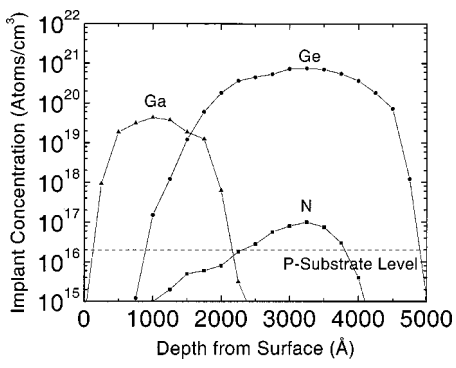

FIG. 1. Implant profile of SiC/SiC:Ge HBT layers simulated using SRIM 2000 software. The *p*-doping level of the substrate is shown by the dashed line.

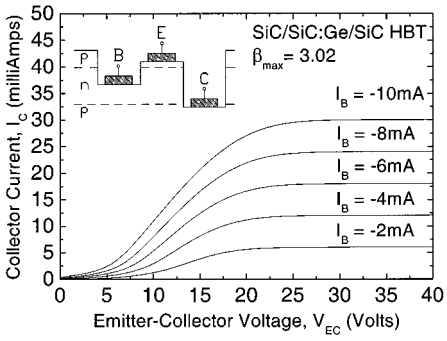

FIG. 2. Common-emitter plot of the collector current vs base–emitter voltage for the HBT, with base current parameter. The emitter–collector offset voltage is approximately 5 V. The peak common-emitter current gain is about 3. Inset shows a side view of the mesa-HBT structure. The $p-n-p$ emitter/base/collector regions have compositions of SiC/SiC: Ge/SiC, respectively. A current of 6.4 mA corresponds to a current density of 100 A/cm^2.

the *n*-type base region. Electron-beam-evaporated titanium was used as the contact to the *p*-type emitter and collector regions. As deposited, the contacts were non-Ohmic, with high series resistance, as verified by current–voltage measurements of the base–collector and base–emitter diodes. A contact anneal was then performed at 925 °C for 10 min in vacuum to lower the contact resistance for devices fabricated after both implant anneals (1050 and 1600 °C). After the contact anneal, the contacts became more Ohmic, the diode $I-V$ characteristics greatly improved, and transistor action was observed. Contact resistance measurements were performed using a transfer length method (TLM) structure. Values for specific contact resistance were from 1 to 2 $\times10^{-3}\,\Omega$ cm^2 for the three contacts.

Transistor measurements were performed using Hewlett Packard 4156 and 4142 parameter analyzers. With the exception of devices on the die periphery, the working device yield was high and the transistor properties were found to be uniform to within a few percent. Table IV contains typical transistor parameters after the implant anneals. After the second implant anneal, the maximum measured common-emitter current gain of the HBT increased from 2.05 to 3.02 (a 50% increase). Figure 2 shows the common-emitter dc characteristic of a typical SiC/SiC:Ge/SiC HBT device. Figure 3 shows the Gummel plot of the collector and base current and corresponding common-emitter current gain versus base–emitter voltage. The SiC BJT devices (without Ge) exhibited an increase in beta from 1.95 to 2.21 after the second implant anneal. A large increase in the Early voltage for both devices was noted after the second implant anneal. In each case, the breakdown voltage (BV_{CEO}) of the devices exceeded 50 V.

The increase in the gain and the Early voltage with incorporation of Ge is similar to effects seen in Si/SiGe/Si transistors.[6] For a transistor with a lower-band-gap material

TABLE III. RIE etch conditions for the HBT mesa etches.

Etch	Pressure (mT)	Power (W)	SF_6 (sccm)	He (sccm)	Time (min)
Emitter	100	100	5	10	9
Base	100	125	5	5	43
Collector	100	150	5	5	38

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in the base, an increase in β by a factor of $\exp(\Delta E_g/k_BT)$ is expected, where ΔE_g is the band-gap reduction. From our observed increase in β values, we calculate a ΔE_g of 8 meV. If one assumes a linear interpolation between the band gaps of SiC and Ge, this shift would correspond to an average Ge fraction of 0.32 at. % (compared to the number of Si–C pairs), which is in excellent agreement with the predicted average Ge fraction of 0.34% from implant simulations.

For a transistor with a gradient in Ge concentration from the base-to-collector junction (provided here by the Gaussian nature of the Ge-implant profile), there will also be an increase in the Early voltage V_A by a factor of $\exp(\Delta E/k_BT)$, where ΔE is the band-gap reduction at the collector side of the base. From our typical measured Early voltage values, we calculate a ΔE of 16.4 meV. If we attribute the increase in V_A to the Ge in the base, the model predicts a base-to-collector Ge fraction gradient of 0.65 at. %. This value is also in excellent agreement with the predicted base-to-collector fraction gradient of 0.70 at. % obtained from SRIM implantation simulations. The simulated implant profiles are shown in Fig. 1.

In conclusion, we have fabricated and demonstrated SiC-based HBT devices, based on heterojunctions of SiC with the SiC:Ge alloy. Functional SiC/SiC:Ge/SiC $p–n–p$ HBTs have been fabricated using ion implantation to establish the base and emitter regions. We have shown that the presence of Ge in the base increases the gain and the Early voltage by as much as 33% over a homojunction BJT fabricated without Ge but otherwise with an identical process. The improvement due to Ge incorporation is attributed to an energy-band offset, which increases the emitter–base carrier-injection efficiency. A common-emitter current gain for the HBT of greater than 3 has been achieved. These results show that SiC:Ge is a promising material for SiC-based heterostructure devices.

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