Current–Voltage Characteristics of High Current Density Silicon Esaki Diodes Grown by Molecular Beam Epitaxy and the Influence of Thermal Annealing

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***Abstract*—We present the characteristics of uniformly doped silicon Esaki tunnel diodes grown by low temperature molecular beam epitaxy ($T_{growth} = 275$ °C) using *in situ* boron and phosphorus doping. The effects of *ex situ* thermal annealing are presented for temperatures between 640 and 800 °C. A maximum peak to valley current ratio (PVCR) of 1.47 was obtained at the optimum annealing temperature of 680 °C for 1 min. Peak and valley (excess) currents decreased more than two orders of magnitude as annealing temperatures and times were increased with rates empirically determined to have thermal activation energies of 2.2 and 2.4 eV respectively. The decrease in current density is attributed to widening of the tunneling barrier due to the diffusion of phosphorus and boron. A peak current density of 47 kA/cm^2 (PVCR = 1.3) was achieved and is the highest reported current density for a Si-based Esaki diode (grown by either epitaxy or by alloying). The temperature dependence of the current voltage characteristics of a Si Esaki diode in the range from 4.2 to 325 K indicated that both the peak current and the excess current are dominated by quantum mechanical tunneling rather than by recombination. The temperature dependence of the peak and valley currents is due to the band gap dependence of the tunneling probability.**

***Index Terms*—Dopant diffusion, molecular beam epitaxy, negative differential resistance, rapid thermal annealing, silicon, tunnel diodes.**

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I. Introduction

TO ADDRESS issues of future device scaling and its limitations, researchers are focusing attention on new quantum devices, suitable for integration into silicon CMOS technology, with increased functionality, packing density and speed [1]–[5]. The negative differential resistance (NDR), bi-stability and high switching speeds associated with the quantum mechanical tunneling of electrons in devices including the Esaki tunnel diode, the resonant tunneling diode (RTD), and the resonant interband tunneling diode (RITD) may be exploitable for future logic, memory and oscillator circuits in computing and wireless communications applications.

Commercially available Si and Ge Esaki tunnel diodes are formed by alloying, a method incompatible with CMOS processing [5]. Few reports on a CMOS-compatible tunnel diode exist in the literature, such as Si and SiGe RITDs grown by molecular beam epitaxy (MBE) [6], [7], as well as p^+-i-n^+ diodes grown by MBE [8] and p^+-i-n^+ diodes combined with delta doping planes [9]. These diodes were grown at relatively low temperatures ranging from 325 to 370 °C. Two important figures of merits of tunnel diodes are the peak to valley current ratio (PVCR) and the peak current density. The highest PVCR for any epitaxially grown CMOS compatible tunnel diode is 4.2 (a $Si/Si_{0.5}Ge_{0.5}$ heterostructure Esaki with delta doping planes), while for an all Si diode it is 2.7 [9]. The addition of Ge to the intrinsic spacer was shown to increase the peak tunneling current as a result of lowering the tunneling barrier. The highest previously reported peak current density for a Si based tunnel diode was 22 kA/cm^2 for a $Si/Si_{0.5}Ge_{0.5}$ RITD grown at 370 °C [7]. For an all Si RITD of equivalent structure and growth conditions, the peak current density was approximately one order of magnitude less [7]. A high current density is important for high speed switching applications where fast charging is necessary.

An obstacle to achieving heavily doped n^+/p^+ epitaxial layers by any technique is the low solid solubility of many electrical impurities (dopants) commonly used for Si. During heavy doping of MBE films, a profound effect is the thermally activated surface accumulation of impurities occurring at conventional Si growth temperatures, resulting in low dopant incorporation and spreading of the dopant profile [10], [11]. Gossman *et al.* reported on a low temperature MBE (LTMBE)

(T_{growth} <300 °C) technique which results in crystalline Si layers with 100% electrical activation of Sb and B up to 6×10^{20} cm^{-3} and 1×10^{21} cm^{-3}, respectively, for layers grown below a critical thickness, $h_{epi}(T)$ [12], [13].

There are disadvantages, however, associated with low temperature growth. Jorke *et al.* observed a significant increase in bulk recombination currents due to mid-gap states for Si diodes grown at 325 °C compared to diodes grown at 500 °C [8]. Several authors have reported high concentrations of point defects [14] or microvoids [15], which were detected using positron annihilation spectroscopy. For example, Gossman *et al.* [14] found a density of vacancy-like defects of $\sim 10^{18}$ cm^{-3} for epitaxial Si films grown at 220 °C, while similar layers grown at 475 °C had a defect density of approximately three orders of magnitude less. However, these authors found that rapid thermal anneals (RTA) above 500 °C for 2 min reduced the defect density of the layers grown at 220 °C to below 5×10^{15} cm^{-3}, which is the sensitivity of the positron measurement.

In this paper, we present the properties of uniformly doped Si p$^+$-i-n$^+$ Esaki type diodes grown by LTMBE at 275 °C. We demonstrated a peak current density of 47 kA/cm^2 in a Si-only tunnel diode, which exceeds any previously reported Si based NDR device fabricated by epitaxy or alloying. We attribute our high current densities to the low growth temperature with high dopant incorporation. The PVCR of the diodes grown using this technique were slightly lower than reported in [8], [9], possibly a result of defects associated with the extremely high doping concentrations in our diodes. We quantitatively discuss the influence of post-growth annealing on the current–voltage (*I–V*) characteristics in the temperature range from 640–800 °C. The tunneling currents at constant biases were shown to decrease upon annealing with a rate characterized by thermal activation energies between 2.2–2.4 eV. *I–V* measurements taken between 4.2–325K revealed that the current is dominated by quantum mechanical tunneling for all applied voltage biases studied in this investigation.

II. Experimental

Uniformly doped Si Esaki diodes were grown by LTMBE in an EPI-620 MBE system. Si was evaporated from an electron gun at a rate of 0.5 nm/minute. P-type (boron) and n-type (phosphorus) dopants were evaporated from an elemental B source and a gettered compound GaP source [16], respectively. A 10-nm intrinsic Si spacer (i = nominally undoped) was grown between the n$^+$ and p$^+$ regions. The substrate temperature during growth was 275 °C, previously calibrated by observing the Au and Al eutetic reactions on a silicon substrate. A 15 nm p$^+$-type Si buffer ($N_A = 1 \times 10^{19}$ cm^{-3}) layer was grown on an 0.01 Ω-cm p-type (001) substrate, followed by the active regions: a 15 nm p^{++}-type Si layer, followed by a 10-nm i-layer, and finally the 30 nm n^{++}-type Si layer. Secondary ion mass spectrometry (SIMS) revealed peak P concentrations of $6 - 8 \times 10^{20}$ cm^{-3} and B concentrations of 4×10^{20} cm^{-3} in the active regions of the diode. The i-layer thickness was calculated from the Si growth rate and does not take into account the possibility of bulk or surface dopant segregation.

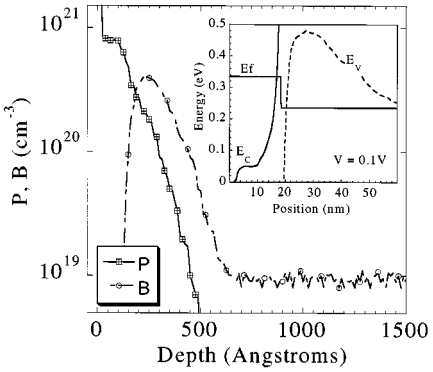

Fig. 1. SIMS profile of B and P dopants for the high current density Si p$^+$-i-n$^+$ Esaki diode prior to *ex situ* annealing. The inset displays the calculated band diagram where E_F is the quasi-Fermi level, E_C is the conduction bandedge and E_V is the valence bandedge.

The samples were annealed *ex situ* in an H_2/N_2 (15%/85%) ambient using a Heatpulse rapid thermal annealing (RTA) furnace. Mesa diodes 15 μm in diameter were formed using standard photolithography and aluminum metallization, followed by junction isolation by etching in a CF_4/O_2 plasma. Room temperature electrical characteristics were measured using a HP4156B semiconductor parameter analyzer.

Samples for low temperature measurements were fabricated using a 40×40 μm^2 square mesa with Ti/Au metallization. Bond pads were formed on top of a polyimide-insulating layer and were subsequently wire bonded into a package compatible with the cryostat. The cryogenic chamber was a Janis Research Inc., model number 14-CNDT Cryostat, and the temperature was controlled using a GaAs temperature sensor (1.4–330K) and a feedback controlled resistive heating element.

III. Results and Discussions

A. Current–Voltage versus Annealing

Fig. 1 displays the SIMS dopant profile for the Esaki diode prior to *ex situ* annealings. The SIMS profile reveals some deviation from the step type dopant profile expected from the growth conditions. It is possible, however, that this concentration spreading is an artifact of the SIMS measurement, since SIMS is known to suffer from knock-on and other effects which limit its depth resolution. Considering this uncertainty, it is difficult to exactly quantify the affects of dopant segregation, which may have occurred during growth. The inset of Fig. 1 displays the simulated band diagram near the junction under 0.1 V bias. The band diagram was calculated by self-consistently solving the effective-mass Schrödinger equation and Poisson equation for the charge profile taken from Fig. 1 (it was assumed that the dopants were completely activated), but does not consider effects such as band-tailing or states within the bandgap. As can be seen from the positions of the quasi-Fermi levels relative to their respective band-edges, the doped layers are highly degenerate with a tunneling barrier width of approximately 4–5 nm.

Fig. 2 displays the room temperature current density versus applied voltage characteristics (J–V) of the Si Esaki diode discussed above, after selected *ex situ* RTA anneals. The left-hand graph shows the J–V characteristics of the diode after 60 s

isochronal RTA anneals. The right hand side shows the J–V characteristics after isothermal annealing at 775 °C. Negative differential resistance is observed for the lower three annealing temperatures (Fig. 2, left) and for the shortest two anneal times (Fig. 2, right). Due to the high current density, unannealed samples burned out before any NDR was observed, even under pulsed measurements. Table I lists the peak and valley current densities and their PVCR. Because of the high current the series resistance in the measurement setup (approximately 6 Ω for unpackaged diodes) shifts the peak and valley currents to higher voltages. Analysis in the remainder of this section corrects the J–V data by removing this IR drop.

The diode currents in Fig. 2 are several orders of magnitude higher than expected from normal diode diffusion current. Jorke observed large deviations from ideal diode current in MBE grown p^+-i-n^+ Si diodes in the same bias range, for i-layer thicknesses of 40 nm and less [8]. They observed negative differential resistance for i-layers of 10 nm and 5 nm. These observations are consistent with earlier studies of alloyed junction Si Esaki diodes [17]–[19], where the current transport below the onset of NDR was shown to be due to phonon assisted tunneling transitions from conduction to valence band states (the band to band tunnel current). The current at, and beyond, the valley voltage, referred to as the excess current, was shown to be due to tunneling through defect levels in the forbidden energy gap up to a voltage where the thermal (i.e., diffusion or recombination) current begins to dominate. Both the band-to-band tunnel current and the excess current are proportional to an effective density of states and the probability for a tunneling transition to occur. The effective density of states for band-to-band tunneling can be expressed as an overlap integral between the density of states in the valence and conduction band multiplied by the occupational probabilities at a given energy [20]. Studies of the effects of high energy electron bombardment on the excess current on Si and Ge Esaki diodes revealed that the excess current increased proportionally to the electron dose [19]. The bombarding electron energy introduced defect energy levels within the material bandgap. Thus, the magnitude of the excess current was proportional to the density of defect states within the gap. The tunneling probability for both the band to band at constant bias and excess tunneling currents are exponentially dependent on effective mass, the barrier height and width, and field strength [20], [21]. Expressions for the band to band tunneling current (J) and the excess tunneling current (J_x) are, respectively, as follows:

$$J = Const \times D \times \exp\{-\beta m^{*1/2} n^{*-1/2} E_G\} \quad (1)$$

$$J_x = Const \times D_x \times \exp\{-(\alpha_x n*^{-1/2}\, e^{1/2}) \cdot (E_G - eV + 0.6(V_n + V_p))\}. \quad (2)$$

The density of defect states is given by D_x, α_x is a material constant, e is the elementary charge, n^* is the effective carrier concentration, E_G is the band gap, V_n and V_p are the quasifermi levels in the conduction and valence bands in volts, and V is the externally applied bias voltage across the junction. Equation (1) is a simplified expression for the band to band tunneling current using the abrupt junction approximation and assuming the junction potential is approximately equal to the bandgap voltage

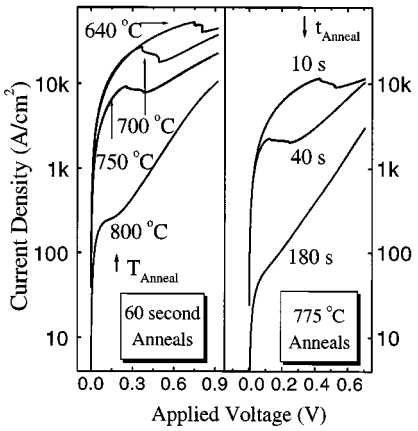

Fig. 2. Current density versus the applied voltage for a LTMBE Si tunnel diode after 60 s anneals at various temperatures (left hand plot). The right hand plot displays the same diode structure after annealing at 775 °C for various times.

[21]. The parameters β and m^* (tunneling effective mass) are constants and D represents the density of states overlap integral at a given bias (β is bias dependent).

For the abrupt junction approximation, the zero bias depletion width (W_0) is inversely proportional to the square root of the effective carrier concentration n^*, defined by

$$\frac{1}{n^*} = \left(\frac{1}{n} + \frac{1}{p}\right) \sim W_0^2 \quad (3)$$

where n and p are the electron and hole concentrations on either side of the junction. Because $n^{*-1/2}$ is proportional to the depletion width, it is referred to as the junction width parameter. The band to band tunnel current and the peak current depend exponentially on $n^{*-1/2}$ [18]. This is a consequence of the exponential dependence of the tunneling probability on the width of the tunneling barrier, i.e., the depletion region.

We determined the effective values of n^* versus annealing temperature for our high current density p^+-i-n^+ Si tunnel diodes by extrapolating the straight-line fit of $\ln(J_{25\ \mathrm{mV}})$ versus $n^{*-1/2}$ in [18, Fig. 2] to our $J_{25\ \mathrm{mV}}$ values (corrected for series resistance). The bias of 25 mV is chosen to be consistent with Logan's data [18], and because at this bias the current transport is expected to be solely due to tunneling between conduction to valence band states; the contribution from the excess or defect current becomes significant only at higher biases. From the results in Table I we note that the effective value of n^* decreases as a function of anneal temperature.

Fig. 3 depicts the natural logarithm of the current density (corrected for series resistance) at 25 mV (closed triangles) and 350 mV (open triangles) versus $1/$

where J_o and r_o are constants, and t_{anneal} and T_{anneal} are the annealing times and temperatures, respectively.

Fitting the data in Fig. 3 to equations (4) and (5) (solid lines) gives values for the activation energy $E_A = 2.24 \pm 0.42$ eV for the current at 350 mV, and $E_A = 2.39 \pm 0.36$ eV for the current at 25 mV. As discussed previously, the current at 25 mV bias is assumed to be dominated by band-to-band tunneling. We assume also that at 350 mV the excess current is due to tunneling through defect levels as in [19]. The latter assumption is further validated in the following section where the current at a constant bias of 325 mV was shown by its temperature dependence to be a tunneling current. From the extracted activation energies and their uncertainties, it is apparent that both tunneling currents (band to band and defect related tunneling current) have nearly the same dependence on thermal annealing. This explains why the PVCR only varies by a factor of 1.5, while the absolute magnitudes of peak and valley currents vary by more than two orders of magnitude over the range of annealing temperatures. We note from (1) and (2) that the one common variable for both the band-to-band current and the excess current is the exponential dependence on the tunnel barrier width [via $n*$ in equations (1) and (2)]. As discussed in more detail below, we conclude that for the annealing conditions used in this study, the change in magnitudes of the peak and valley currents are due to broadening of the tunnel barrier which occurs for anneals above 640 °C.

Duschl *et al.* has recently reported on the dependence of the peak and valley current on one minute anneals in the temperature range from 550 to 750 °C for heterostructure/delta doped Si/$Si_{0.5}Ge_{0.5}$ p^+-i-n^+ tunnel diodes [9]. These authors observed two trends in the post annealing *J–V* characteristics, where we distinguish between the low temperature (<680 °C) and high temperature (>680 °C) behavior. As the annealing temperature was increased from 550 to 680 °C, the peak current of the Si/$Si_{0.5}Ge_{0.5}$ tunnel diode remained essentially constant, while the valley current decreased. In this temperature region, the PVCR increased from approximately 1 to the maximum value of 4.2 for a 680 °C anneal. These authors attributed this behavior to the annealing of electrical active point defects, which were formed during low temperature growth. A reduction in the number of these defects will decrease the density of defect states [D_X in (2)]. Justification of their conclusion may be found in [14] where the density of vacancy-like defects in Si epitaxial layers grown by LTMBE was reduced by three orders of magnitude after annealing above 500 °C [14]. However, no activation energy was reported for either study. Previous authors have correlated the annealing dependence of excess currents in alloyed junction Si Esaki diodes with a decrease in point defects. Logan *et al.* [23] examined the effect of electron induced damage to the lattice on the excess current and the effects of post-bombardment annealing. Annealing at temperatures from 300–400 °C reduced the excess current to its pre-bombardment magnitude at a rate characterized by an activation energy of 1.3 eV. The increase/decrease in excess current was attributed to the creation/annihilation of defect states within the bandgap [i.e., an increase/decrease of D_X in equation (2)]. During these electron irradiation/annealing experiments, the peak current remained nearly constant, indicating that the width of the tunnel barrier was essentially unaffected during irradiation/bombardment.

TABLE I
ANNEALING DEPENDENCE OF SI ESAKI DIODE ELECTRICAL PROPERTIES FOR ONE MINUTE ANNEALS. THE VALUES WERE AVERAGED FOR FIVE DIODES AND THE STANDARD DEVIATION IS GIVEN. THE VALUES OF THE REDUCED CARRIER CONCENTRATION, n^* WERE EXTRAPOLATED FROM THE DATA GIVEN IN [18]. * THE DIODE ANNEALED AT 800°C DID NOT EXHIBIT NEGATIVE DIFFERENTIAL RESISTANCE

Anneal Temperature °C	J_{peak} (kA/cm^2)	J_{valley} (kA/cm^2)	PVCR	Extrapolated n^* ($\times 10^{19}$ cm^{-3})
640	46.8 ± 3.1	35.8 ± 1.0	1.3 ± 0.06	4.9
680	43.4 ± 1.9	29.2 ± 1.3	1.47 ± 0.05	4.8
700	26.1 ± 0.7	18.4 ± 1.3	1.425 ± 0.06	4.4
720	19.0 ± 1.9	14.1 ± 1.2	1.34 ± 0.04	4.0
750	9.3 ± 0.2	7.9 ± 0.09	1.17 ± 0.01	3.7
775	3.6 ± .05	3.2 ± 0.06	1.1 ± 0.01	3.5
800	0.05*	-	-	2.2

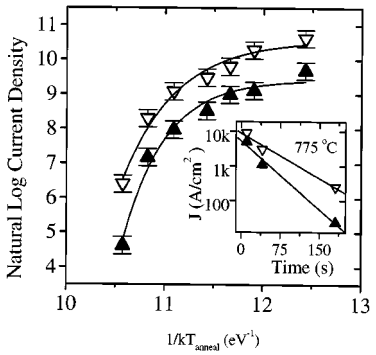

Fig. 3. Natural logarithm of current density versus the inverse of the annealing temperature (T_{ann}) at constant biases and for 60 s anneals, where k_B is the Boltzmann factor. The open triangles represent the current at 350 mV, while the filled triangles represents the current at 25 mV after series resistance corrections. The data was fit to equations (4) and (5), giving an activation energy of 2.24 eV ± 0.42 eV and 2.39 ± 0.36 eV. The inset to Fig. 2 shows the decrease in current as a function of isothermal annealing time.

For annealing temperatures of 680 °C and above (the high temperature region), Duschl *et al.* found that the peak and valley currents decreased at the same rates and more rapidly than for the low temperature anneals [9]. They attributed the decrease to a broadening of the depletion zone due to smearing of both the B and P delta doping spikes, which was confirmed by SIMS.

The high current density Si Esaki diodes that we investigated in this article were annealed under conditions similar to the high temperature anneal region in [9]. From the nearly equivalent thermal dependencies of the band-to-band and the excess currents, we concluded that the dominant mechanism occurring during *ex situ* annealing was the broadening of the tunnel barrier width, which is consistent with Duschl's conclusions for their P and B doped tunnel diodes. For our uniformly doped p^+-i-n^+ Si Esaki diodes, we expect that the broadening of the tunneling barrier is due to dopant diffusion from the heavily doped p^+ and n^+ layers into the intrinsic spacer layer. Using the abrupt junction approximation, we calculated the relative changes in the tunnel barrier width in terms of the extrapolated n* values

listed in Table I. We then approximated a characteristic redistribution length of P and B into the intrinsic spacer using the diffusion data for P and B given in [24] and the solution of the diffusion equation for a pair of semi-infinite solids [25]. For all annealing conditions, the change in the tunnel barrier width determined from the extrapolated $n*$ values were in reasonably good agreement with those values calculated for the characteristic redistribution length of the P and B dopants. Based on the decrease in the 25 mV tunneling current from the value at 640 °C to that after 1 min annealing at 680 °C (800 °C), the values of $n*$ in Table I correlated to an increase of 2 Å (25 Å) in barrier width respectively. Calculations for the relative redistribution lengths for both P and B summed together are ~2 Å (20 Å) for one minute anneals at 680 °C (800 °C).

The origin of the activation energy empirically determined from Fig. 3, may now be correlated with the diffusion of dopants from the n^{++} and p^{++} active regions into the intrinsic spacer layer. From the preceding paragraph, the dependence of the depletion width on the annealing conditions may be given by

$$W = W_{oi}\left(1 + \Theta\sqrt{Dt}\right) \tag{6}$$

where

W_{oi}	initial depletion width before annealing;
t	anneal time;
D	thermally activated diffusion coefficient for dopant redistribution;
$D = D_o \exp(-\Delta/k_B T)$	($D_o$constant and Δ effective activation energy for dopant diffusion);
$(Dt)^{1/2}$	characteristic re-distribution length;
Θ	constant of order unity.

Since tunneling current is exponentially dependent on the width of the tunneling barrier, we derive an expression for the temperature dependence of the tunneling barrier from equation (6) as follows:

$$J(T) = J_{oo} \exp\left\{-\gamma\sqrt{D_o t}e^{-(\Delta/2k_B T)}\right\} \tag{7}$$

where γ is a constant. Comparing (7) to (4) and (5) to determine the empirical activation energies for the rate of decay of the tunneling current, we see that our empirical activation energy corresponds to a value of $\Delta \sim 4.4 - 4.6$ eV. For high impurity concentrations, the diffusivity of a dopant in Si is most accurately described by a sum of the various impurity-vacancy interaction components, each with its own activation energy and concentration dependent pre-factors [26]. For most group III and IV elements in Si, these activation energies are between 3.5 and 4.5 eV. We note that the activation energy given in [26], which is close to our empirically determined value of −4.5 eV, is for the diffusion of P via a doubly ionized acceptor type vacancy with Δ =4.37 eV.

The optimal anneal temperature for high PVCR in our study, as well as that in reference [9], is 680 °C. This temperature should correspond to that where defect annealing is most rapid, however; it is still low enough to prevent dopant redistribution from increasing the barrier width; thus the peak current remains essentially constant. The use of dopants with lower diffusivities, such as Sb and As, may permit higher temperature stability of

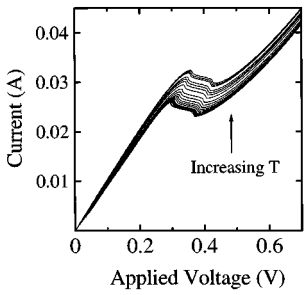

Fig. 4. Variable temperature *I–V* curves of a 40×40 μm^2 Si Esaki tunnel diode after a 60 s anneal at 775 °C. Measurement temperatures ranged from 4.2 to 325 °K. The variation of peak voltage versus peak current yields a series resistance of 8 Ω.

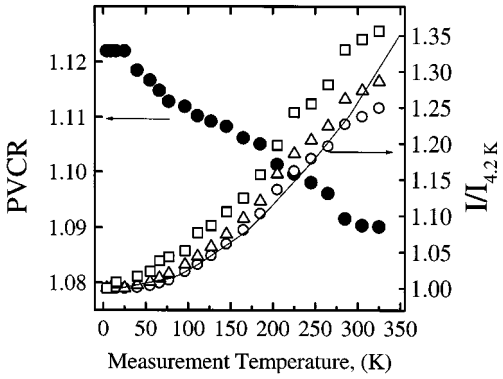

Fig. 5. Peak-to-valley current ratio (PVCR) of the diode from Fig. 4 as a function of measurement temperature (filled circles, left axis). The right axis shows the correct scale for the ratio of the peak (open circles) and valley (open triangles) currents as well as the current at a constant bias of 325 mV (open squares) normalized to their respective current values at 4.2 K. The solid line is a fit to (8) using the optical bandgap data of reference [24], illustrating that the temperature dependence of the tunneling current is due to the change in bandgap in the tunneling probability.

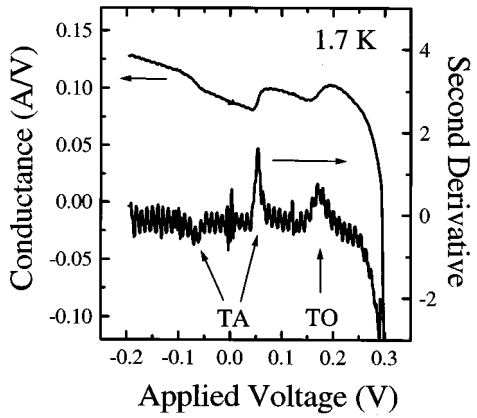

Fig. 6. Conductance, dI/dV (left axis) and the second derivative, d^2I/dV^2 (right axis) of the LTMBE grown Si Esaki diode from Fig. 4 taken at 1.7K. After correcting for series resistance, we attribute the inflections to contributions from the TA (18.4 meV) and TO (57.6 meV) phonons to the tunneling current.

We have fit the temperature dependence of the peak current ratios to the above equation using the optical bandgap temperature dependence data of [28] to obtain the solid line shown in Fig. 5. A value of 5.1 eV^{-1}

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