Fitting Optical Interconnects to an Electrical World- Packaging and Reliability Issues of Arrayed Optoelectronic Modules

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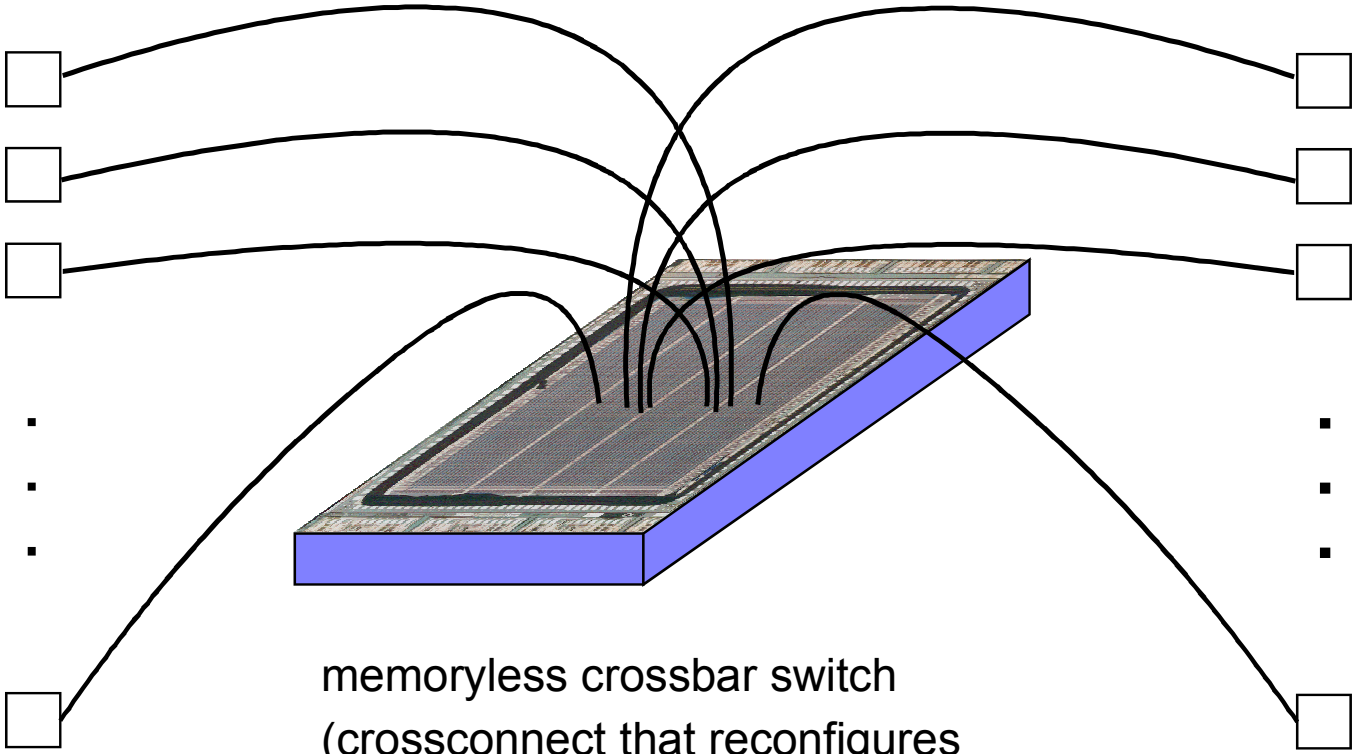
OUTLINE

1. Technology
    a. Physical rack limitations on optical interconnects dictating a bent package.
    b. Optical packaging difficulties encountered going to 2-dimensional optics.
    c. Reliability limitations on the data rate of VCSEL's and possible alleviation via either revolutionary thermal device packaging or modulators.
2. Market path

Early experiments: The Bell Labs photonic switch; systems with no electrical data lines going into the photonic chip, only optical in/out

Construction of large system by interconnecting of small electrical systems through fiber optics via photonic chip

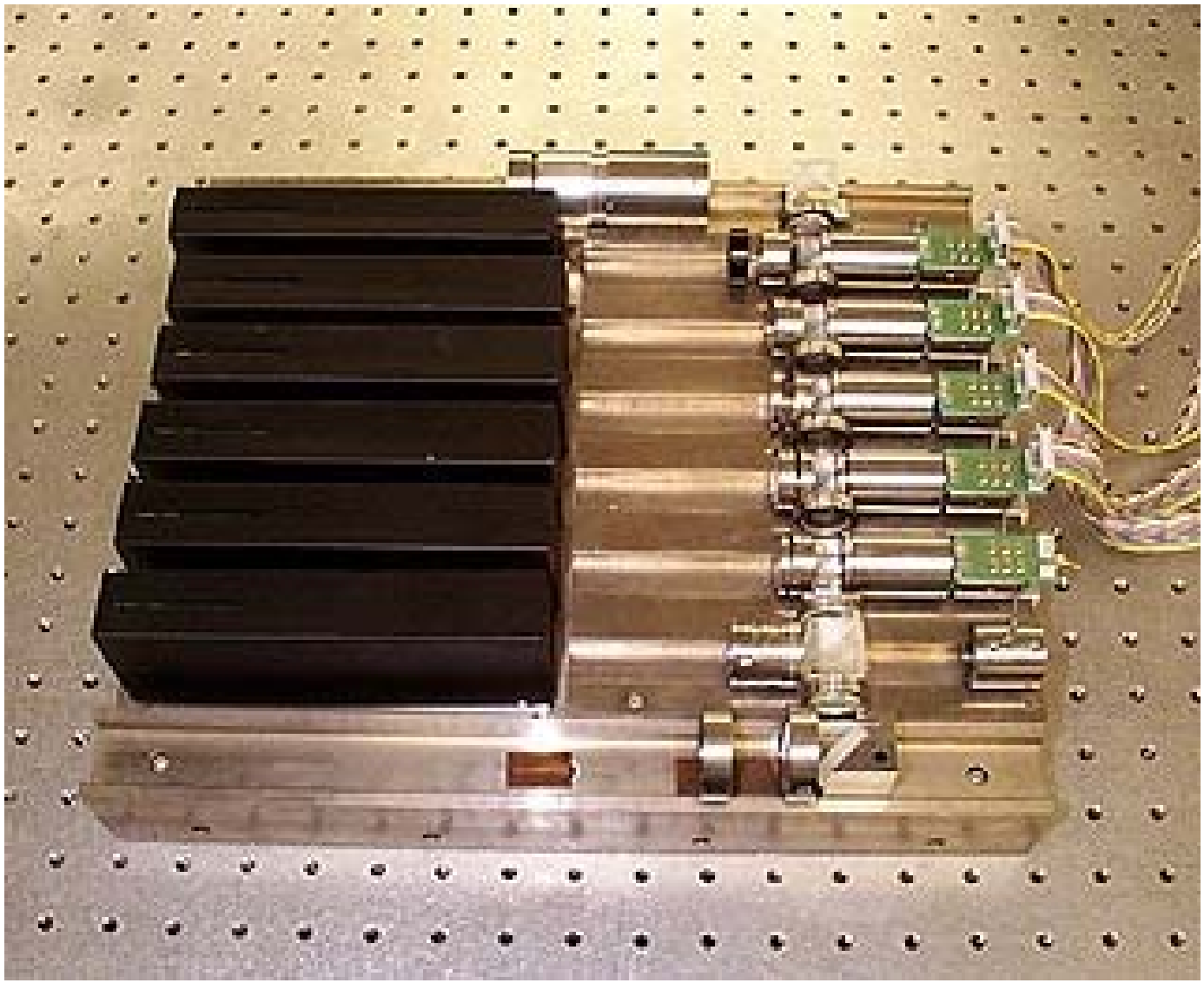


buffered electronic switches

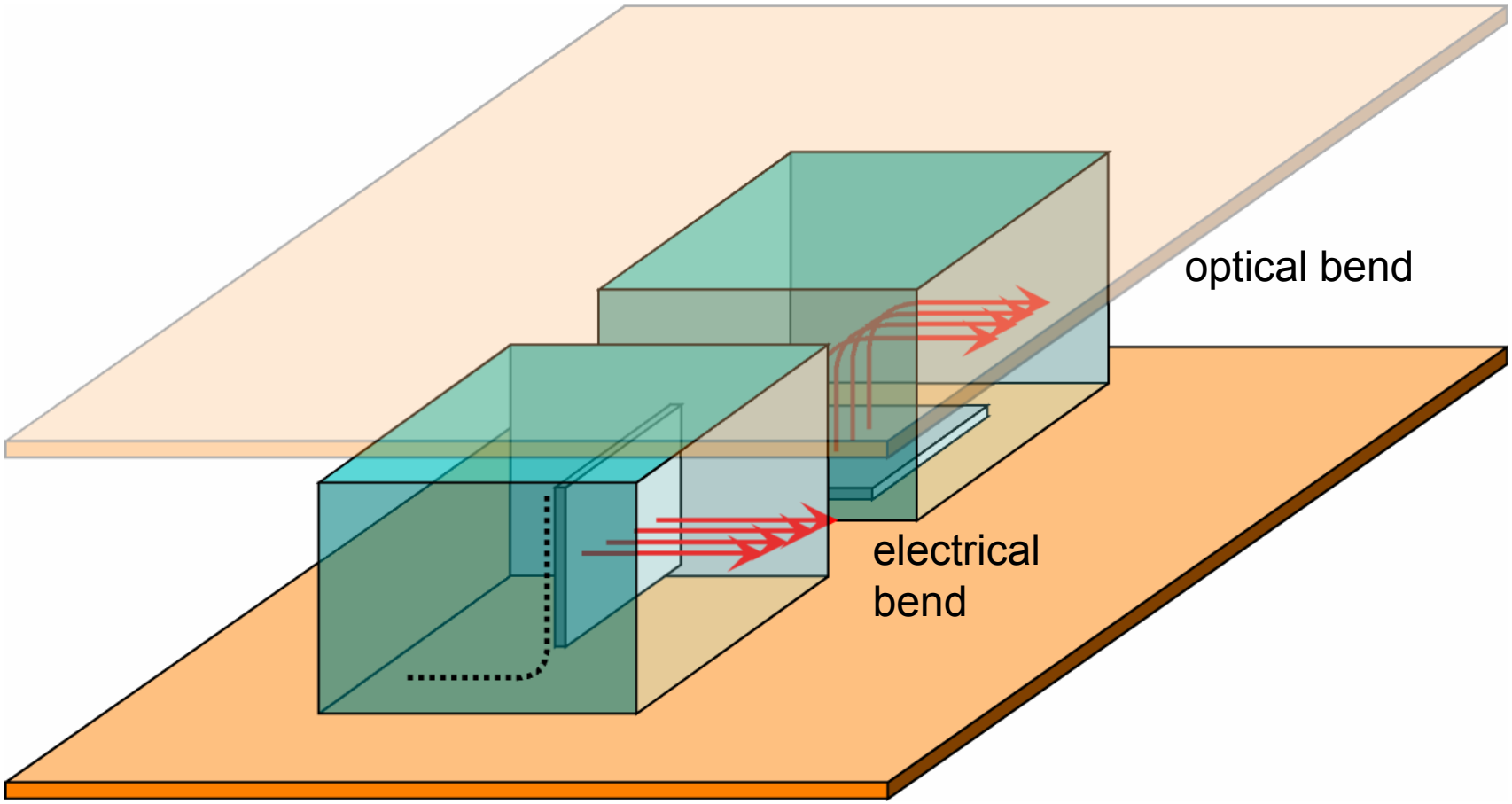
memoryless crossbar switch (crossconnect that reconfigures at the packet rate)- optical data in, optical data out; control for setting switch inputted electrically

buffered electronic switches

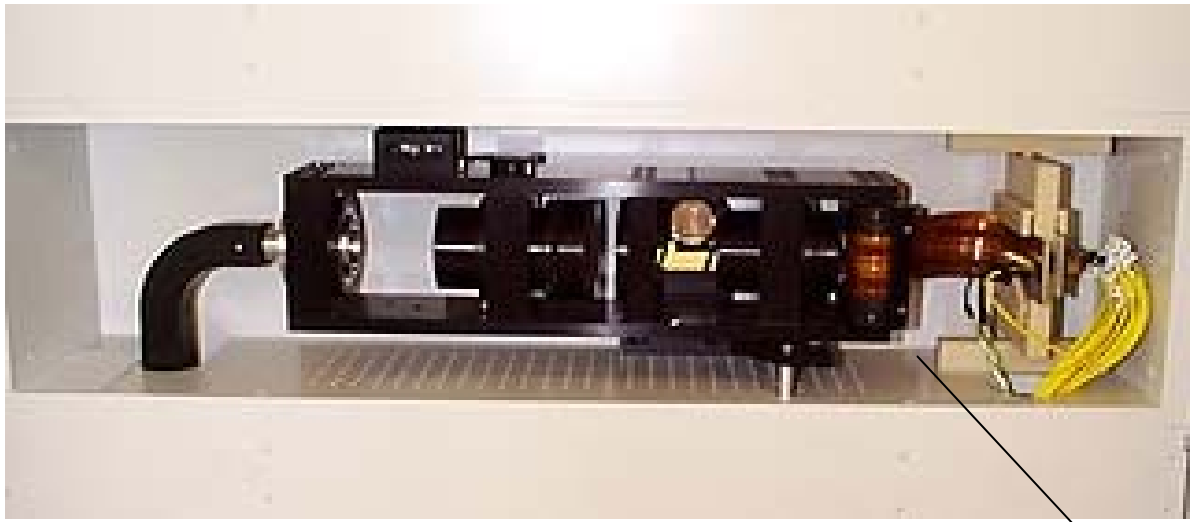
Early experiments: Made without concern of physical constraints in the third dimension, ignoring rack-based system packaging



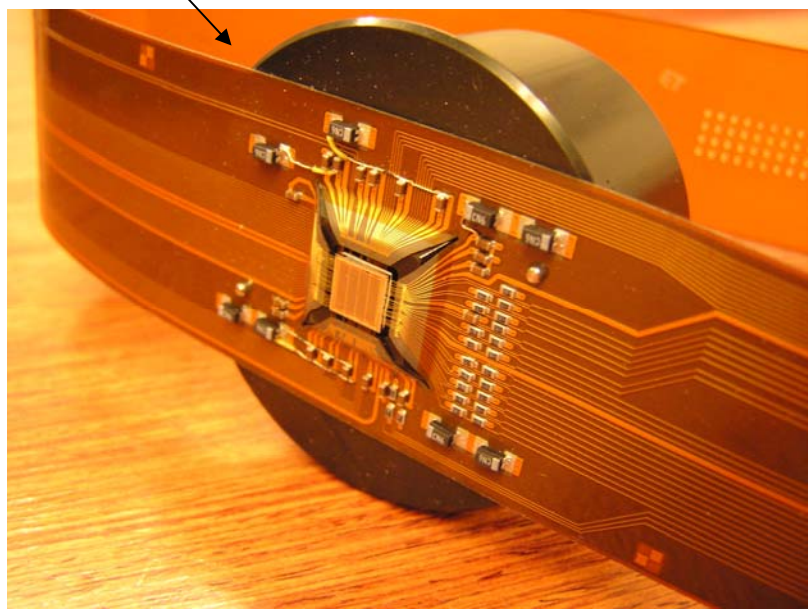
Conforming to existing rack packaging requires the light to come out parallel to the board



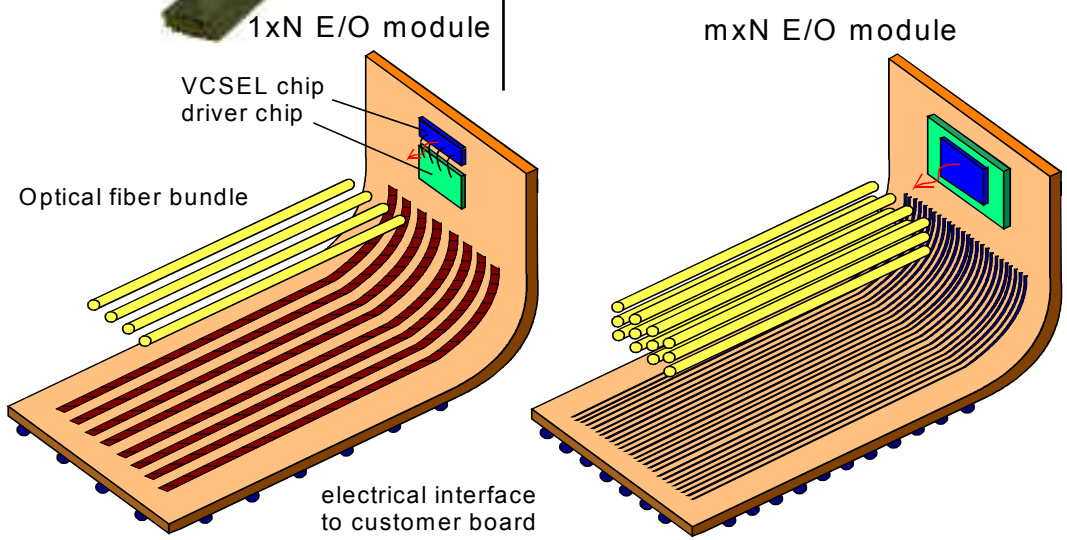
Actually, the later Bell Labs experiments did recognize the need for rack packaging, but with ~ 4 inch clearance requirements (for 4352 channels!)



Used flexible circuit board to effect ninety degree turn of control information inputted electrically to switching chip



Conforming to rack architecture requires using modules, which become harder to make as channel count increases



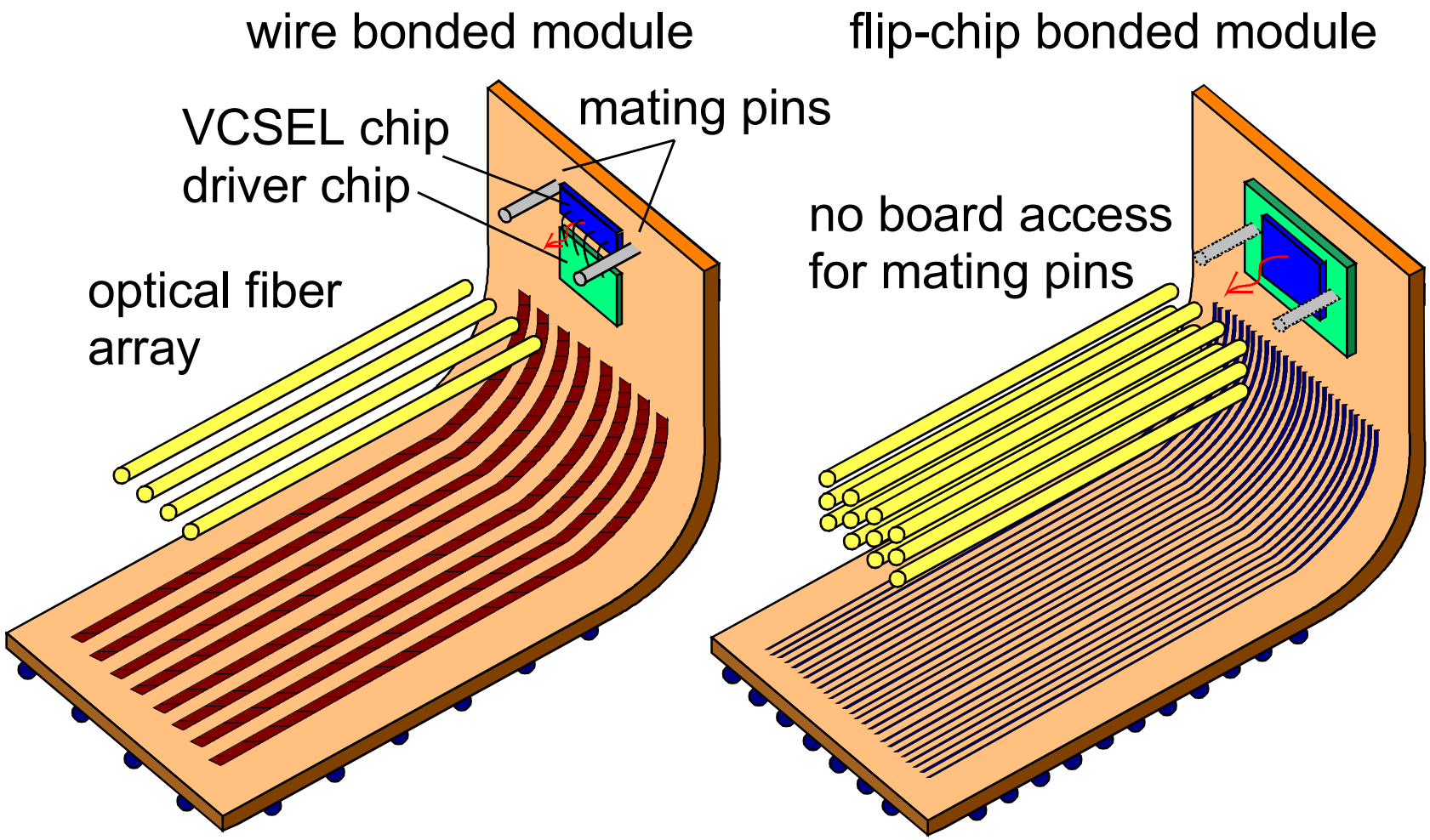
Size of parallel optic modules is actually determined by electrical and thermal considerations!

Since optical pitch is 0.25 mm, but electrical pin or ball pitch to customer board is ~ a millimeter (note: two per signal), electrical footprint increases far faster then optical “footprint” (~ 16x).

Heat sink requirements increase footprint even faster (~ 200x).

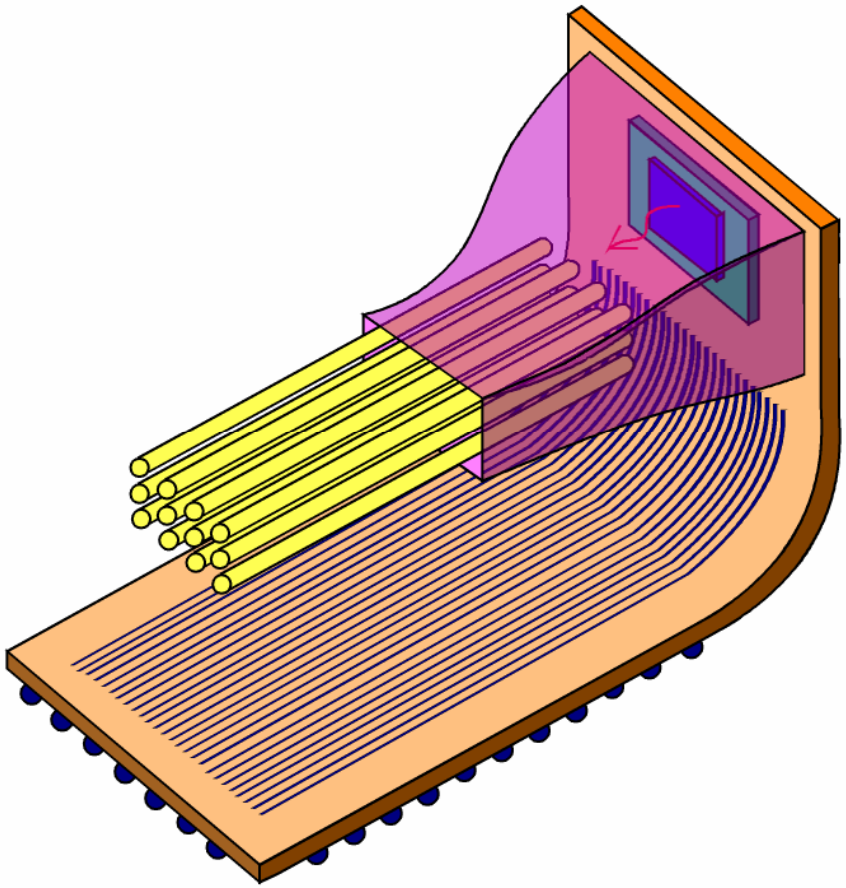
Modules larger than ~ 50-100 channels will require water cooling.

1x12 vs. 2D array packaging: traditional mating pin technique inhibited by chip



2D array packaging: Various approaches for optical packaging

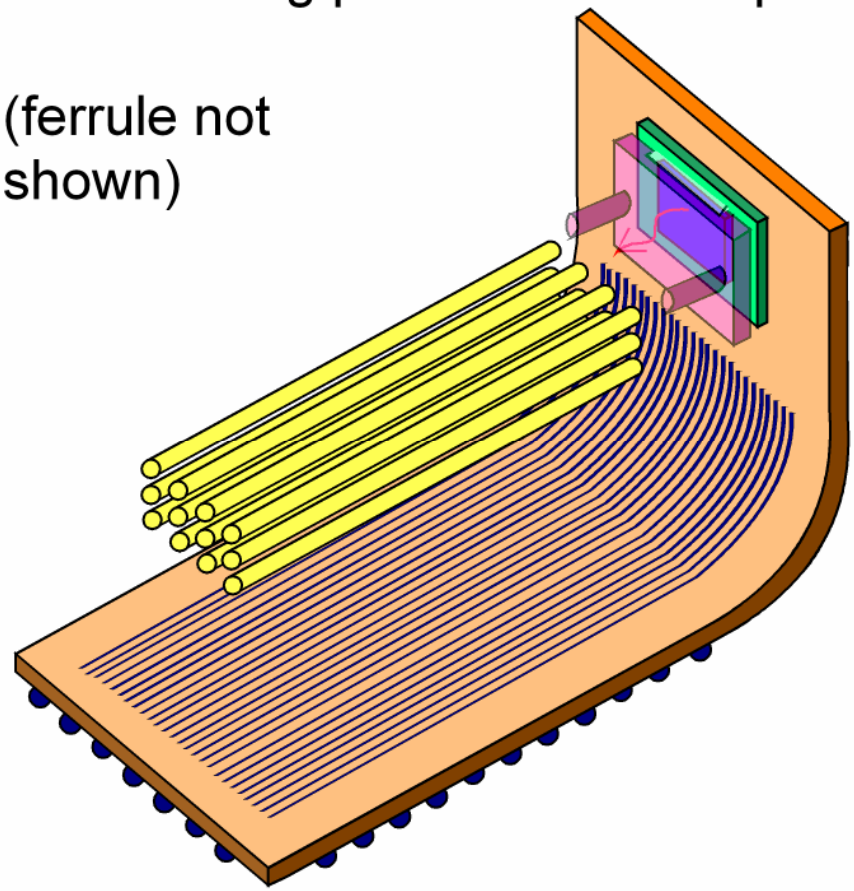
Aralight approach: ferrule mating part affixed to board



A.V. Krishnamoorthy, et al, to appear in IEEE J. Selected Topics in Quantum Elec. (2004).

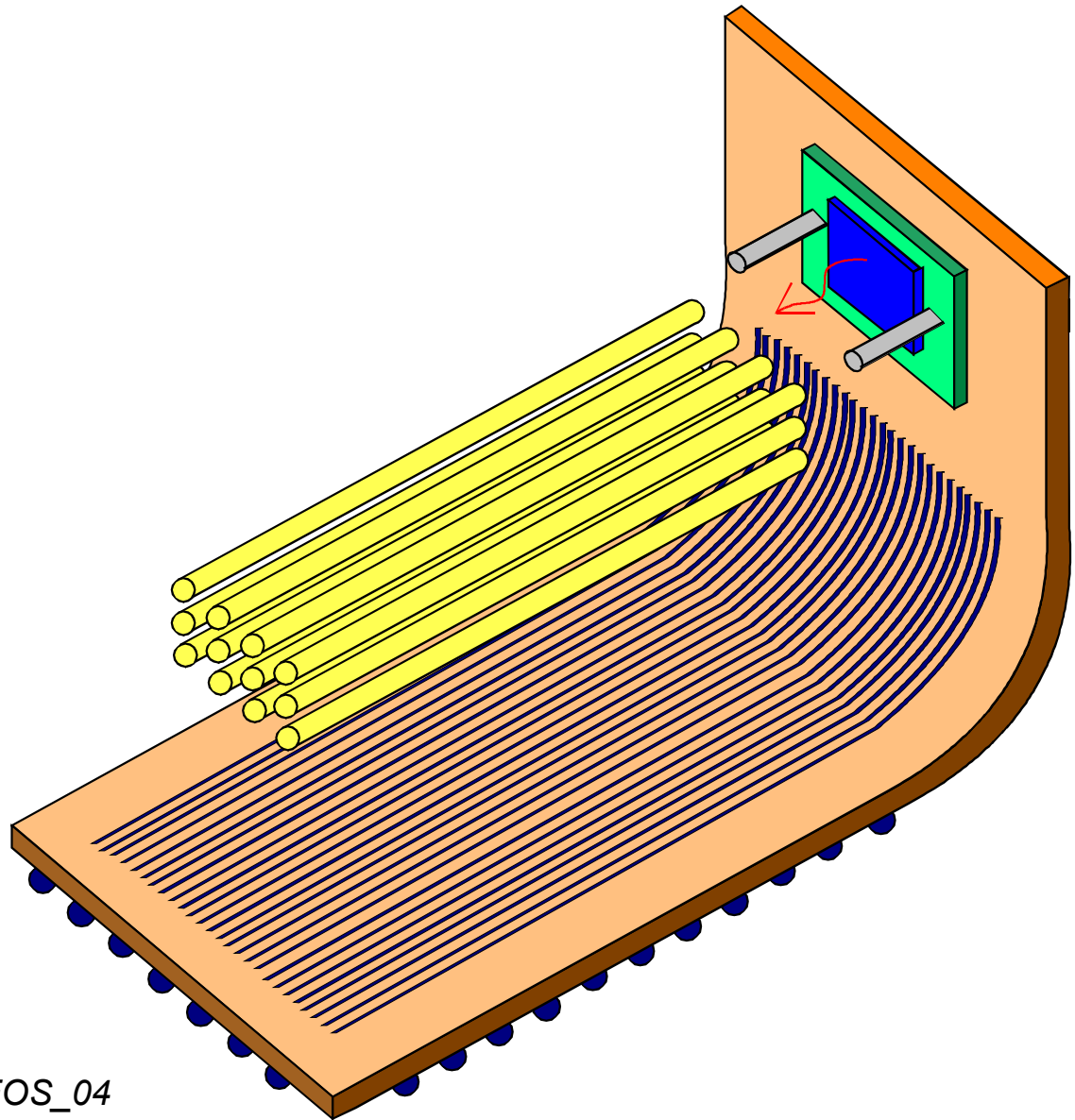
Agilent approach: ferrule mating part affixed to chip

(ferrule not shown)



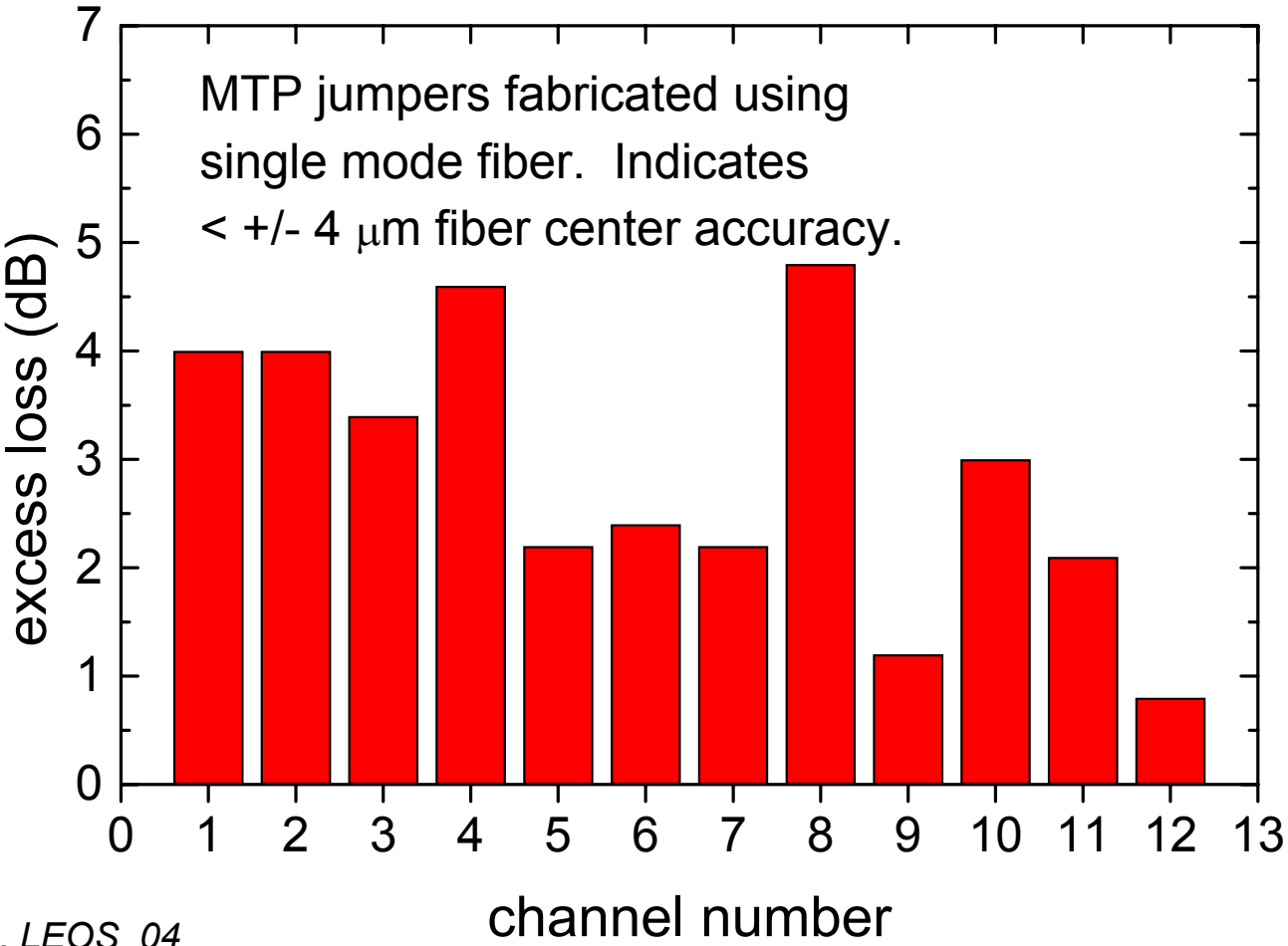
L. Buckman Windover, et al, to appear in the J. Lightwave Tech., spec. issue on Opt. Int. (2004).

2D array packaging: Can the mating pins protrude through holes in the chip?



2D array packaging via protruding mating pins- die placement + fiber-pin accuracy must be less than ~ 10 microns for multimode

Experiment with single mode ribbon mating indicates that injection molded plastic ferrules have < +/- 5 micron accuracy. Must have micron die placement accuracy for protruding mating pin 2D array packaging.



VCSEL reliability: the data (Honeywell) can be modeled effectively

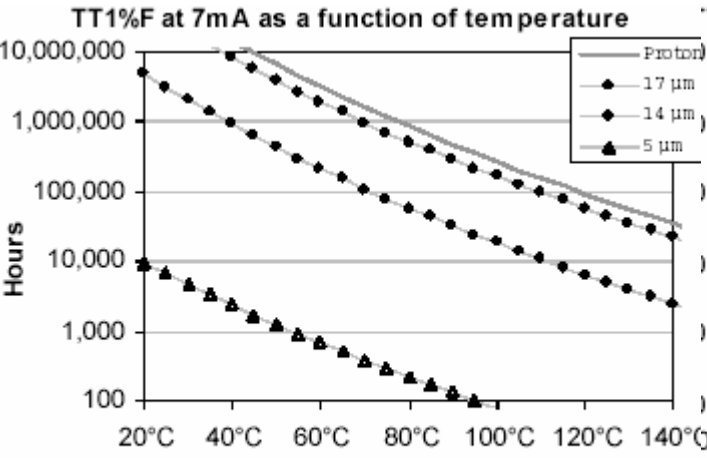
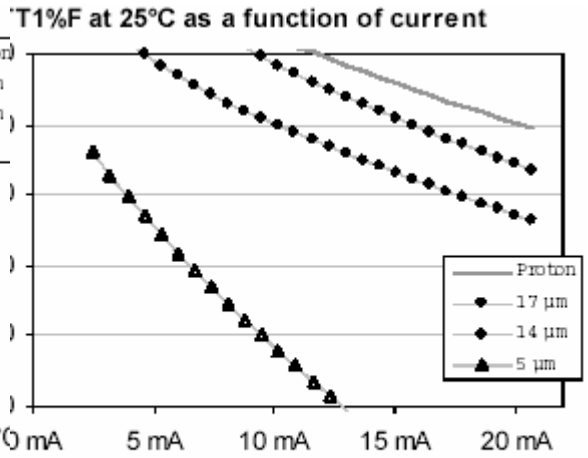
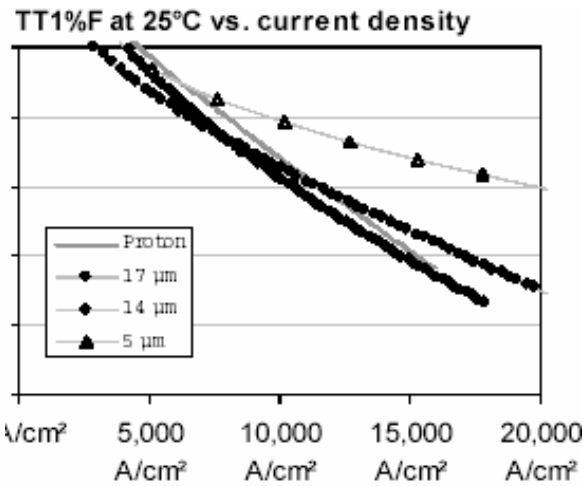


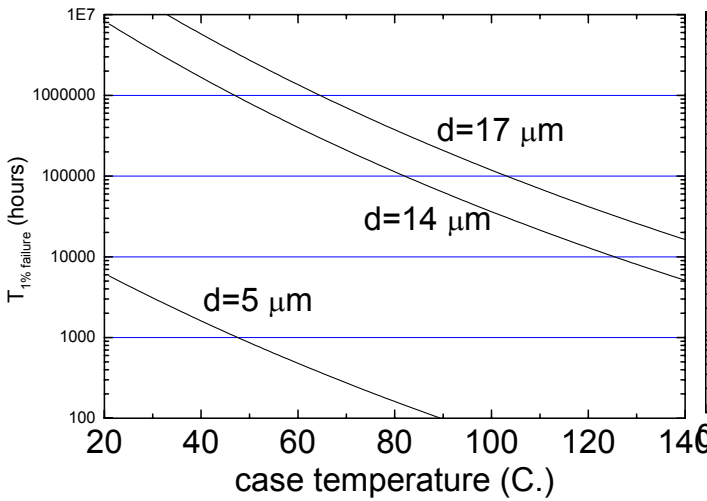
Figure 3. Reliability as a function of ambient temperature at a fixed current.

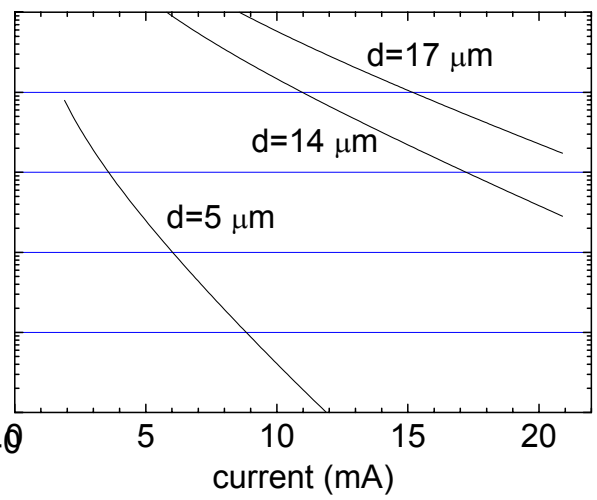


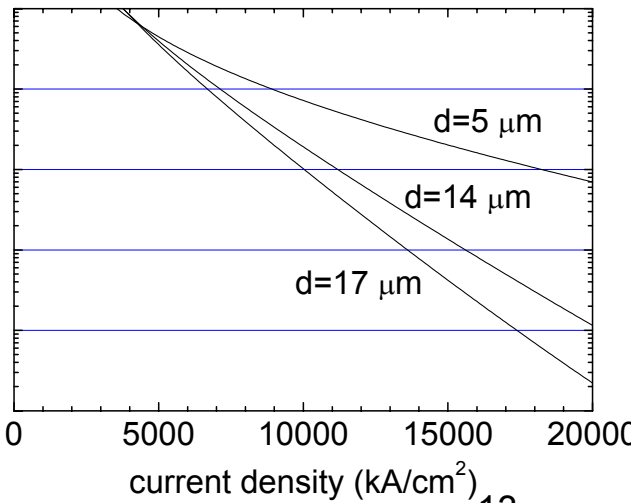
Reliability as a function of current at a fixed re.



Reliability as a function of current density.







VCSEL reliability: the data can be modeled effectively

$$MTF = \frac{A}{j^2} e^{\left(\frac{E_A}{k}\right)\left(\frac{1}{T_j} - \frac{1}{373}\right)}$$

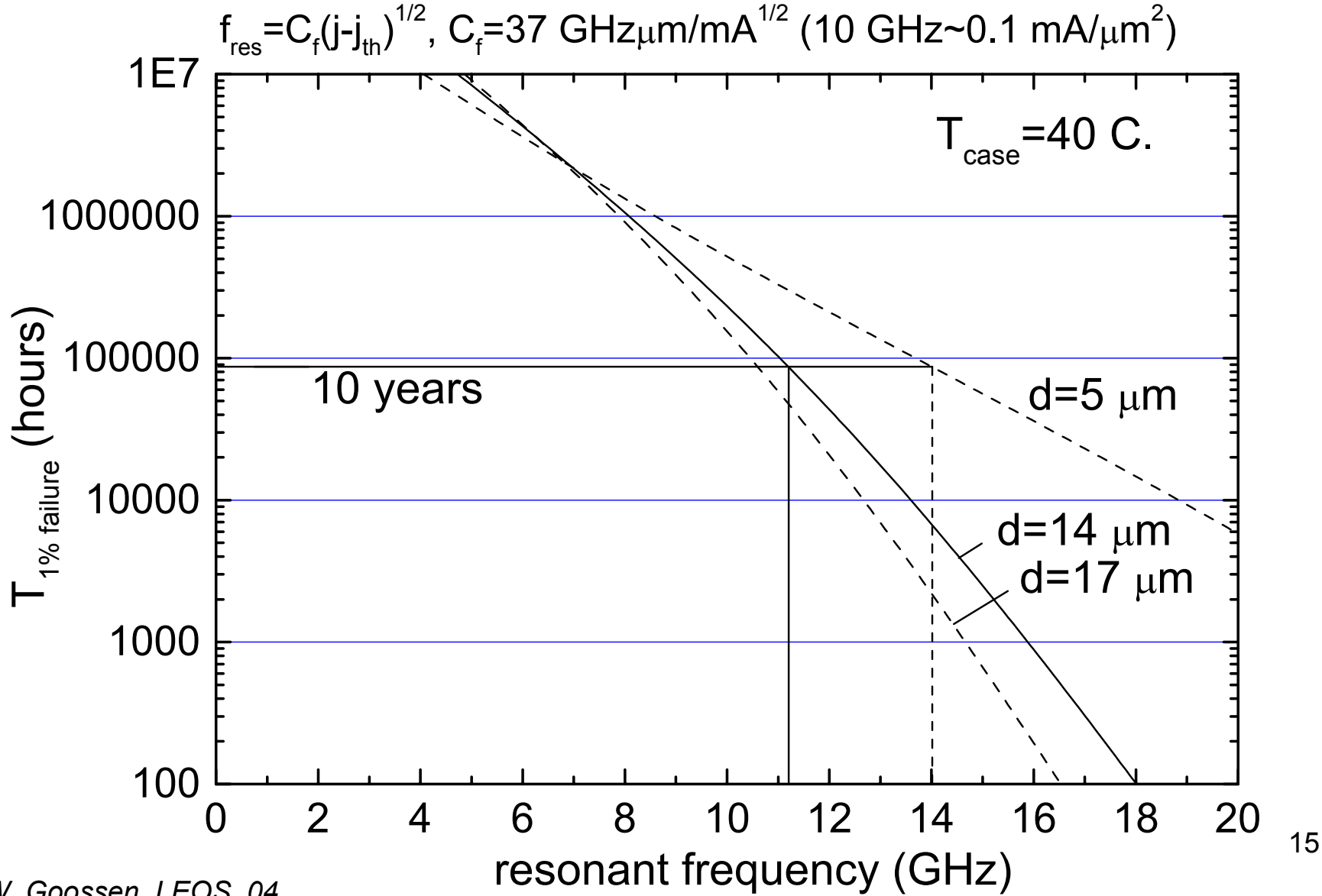
For latest Honeywell data, A=1200

$$T_j \cong T_c + ZIV$$

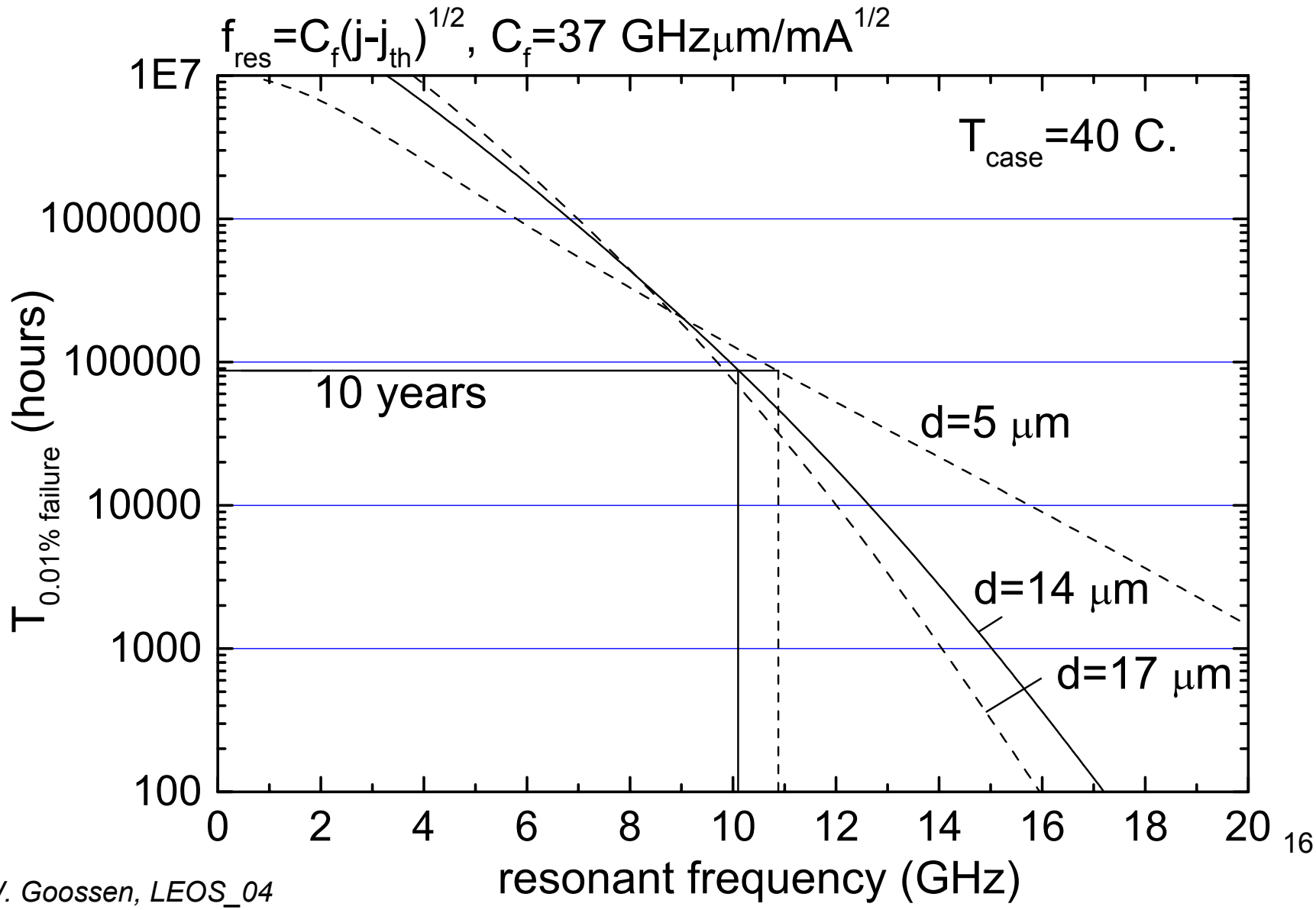
$$MTF \cong \frac{A}{j^2} e^{\left(\frac{E_A}{373k}\right)} e^{\left(\frac{E_A}{k}\right)\left(\frac{1}{T_c + ZIV}\right)} \cong \frac{A}{j^2} e^{\left(\frac{E_A}{373k}\right)} e^{\left(\frac{E_A}{kT_c}\right)} e^{\left(-\frac{E_A}{kT_c^2} ZIV\right)}$$

$$= \frac{65A}{j^2} e^{\left(\frac{ZIV}{12}\right)}$$

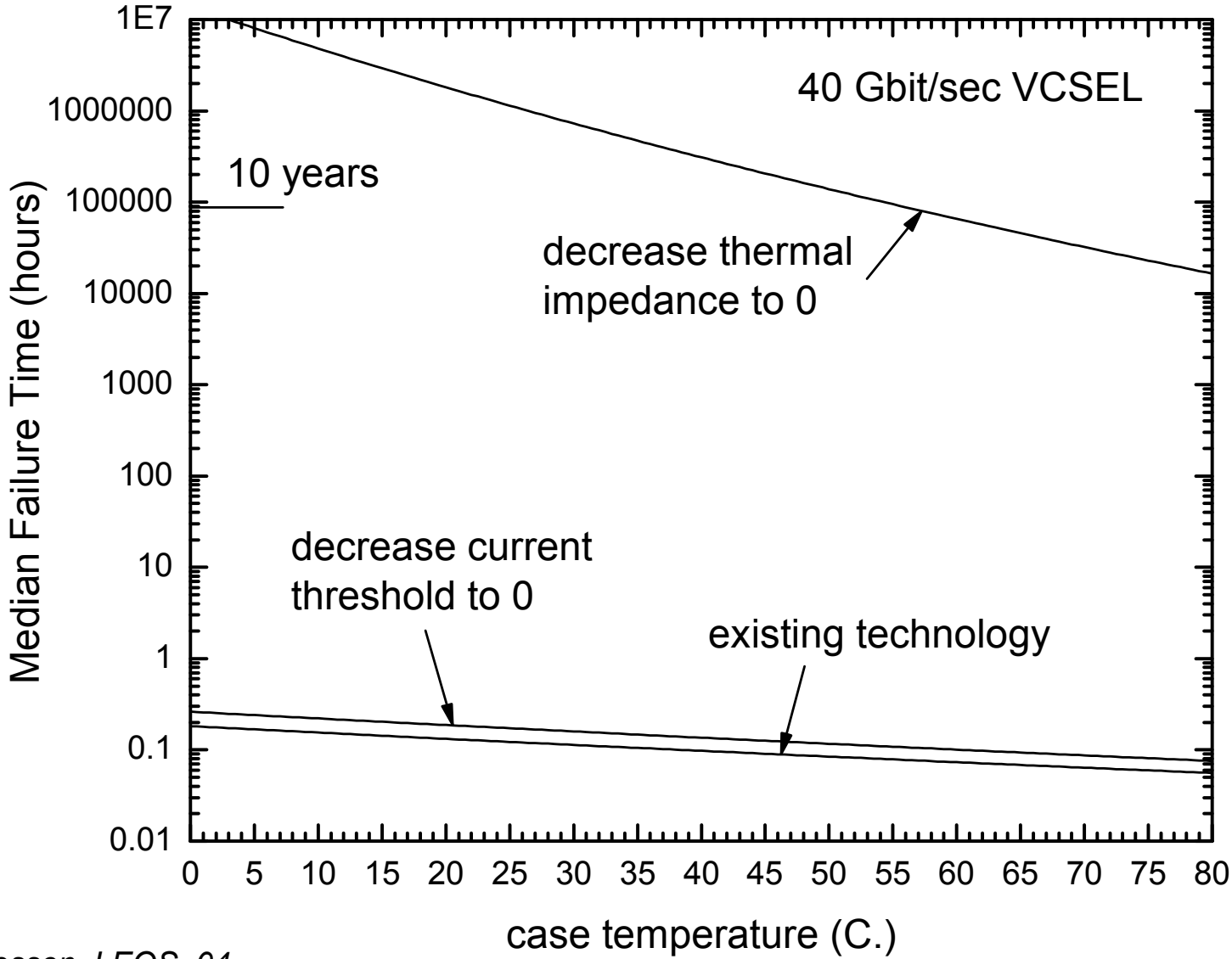
VCSEL reliability: modeling indicates trouble at high data rates



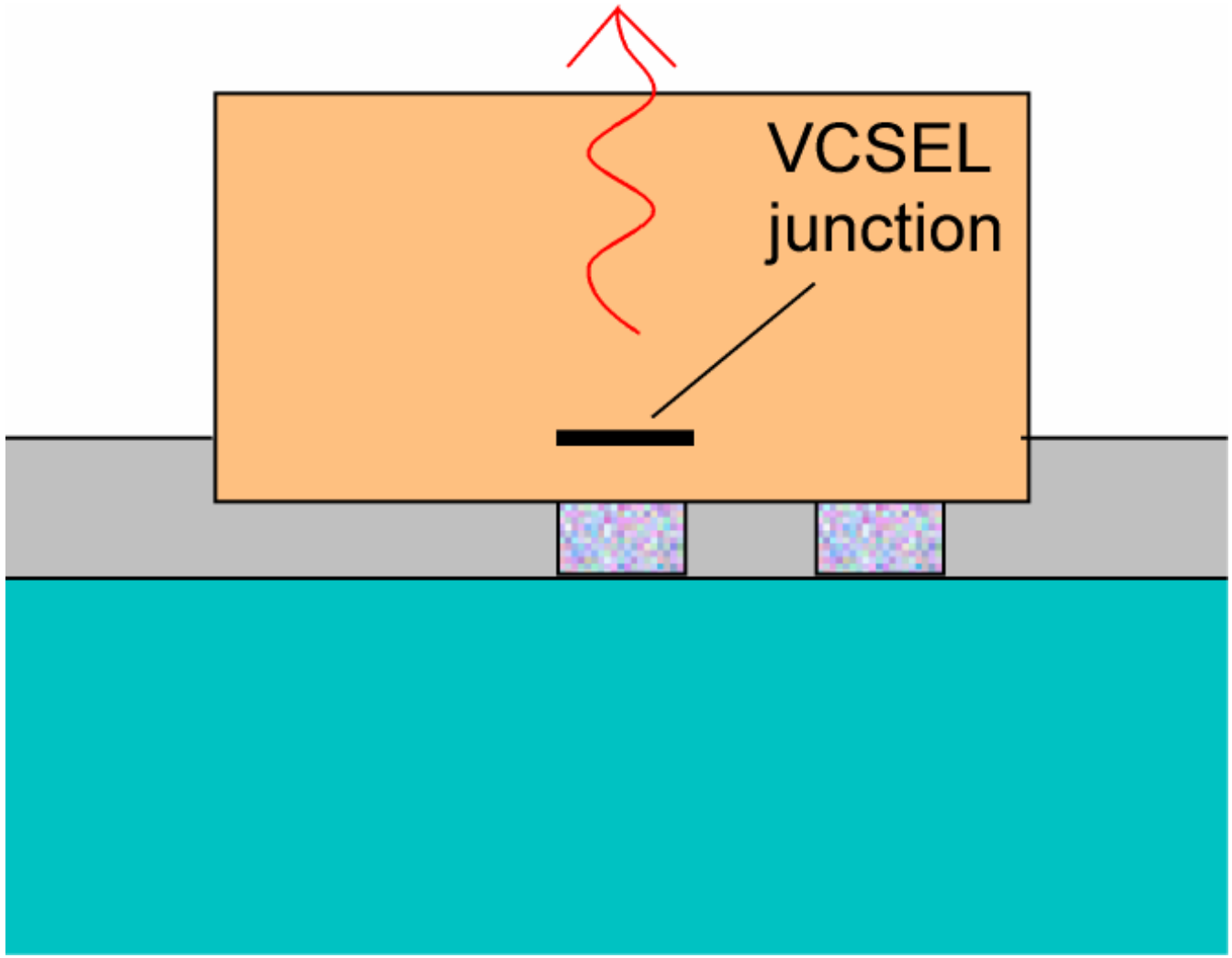
VCSEL reliability for 10000 count array- looks fine at low data rates



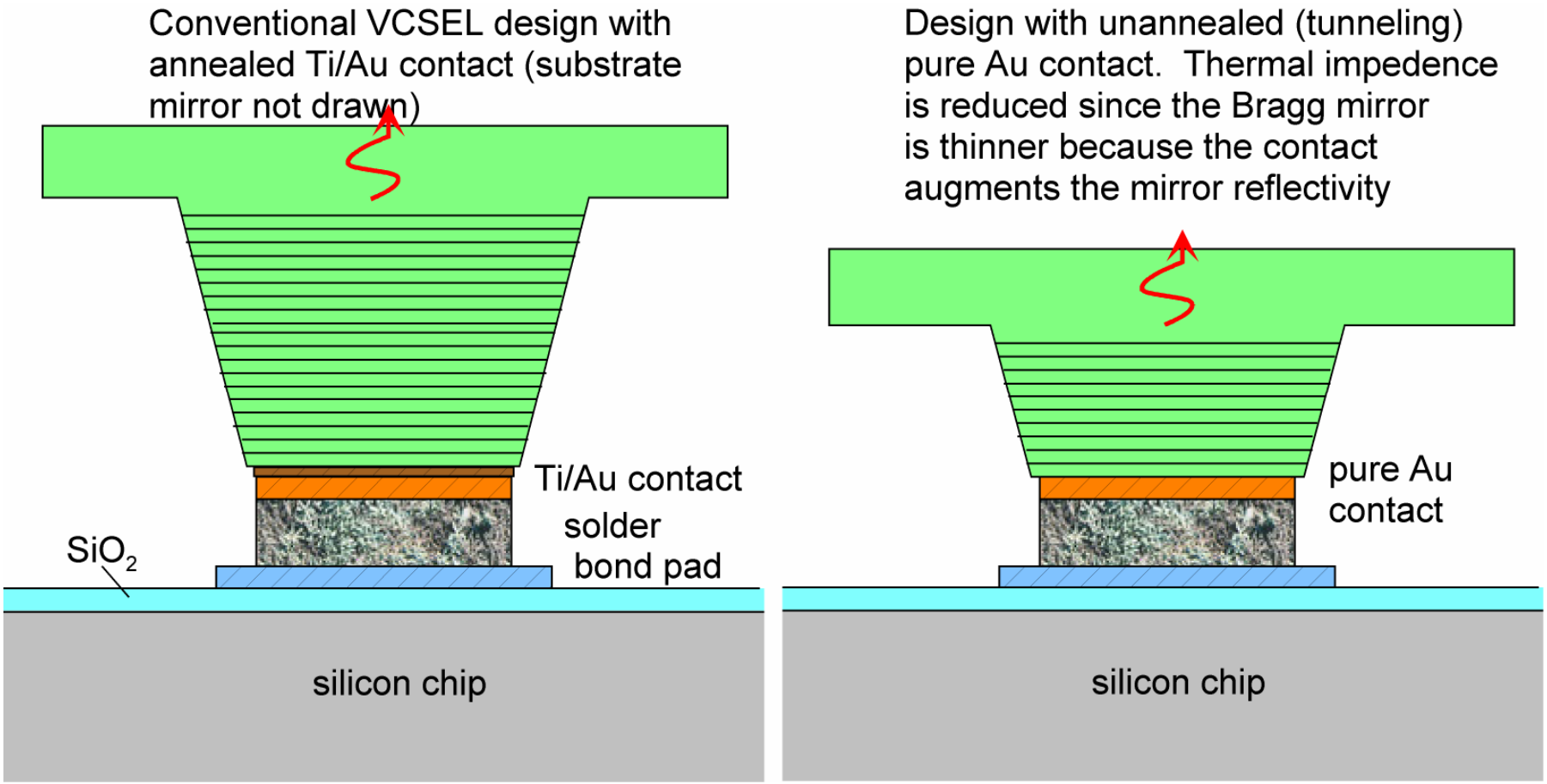
VCSEL reliability can be high if thermal impedance is reduced to zero



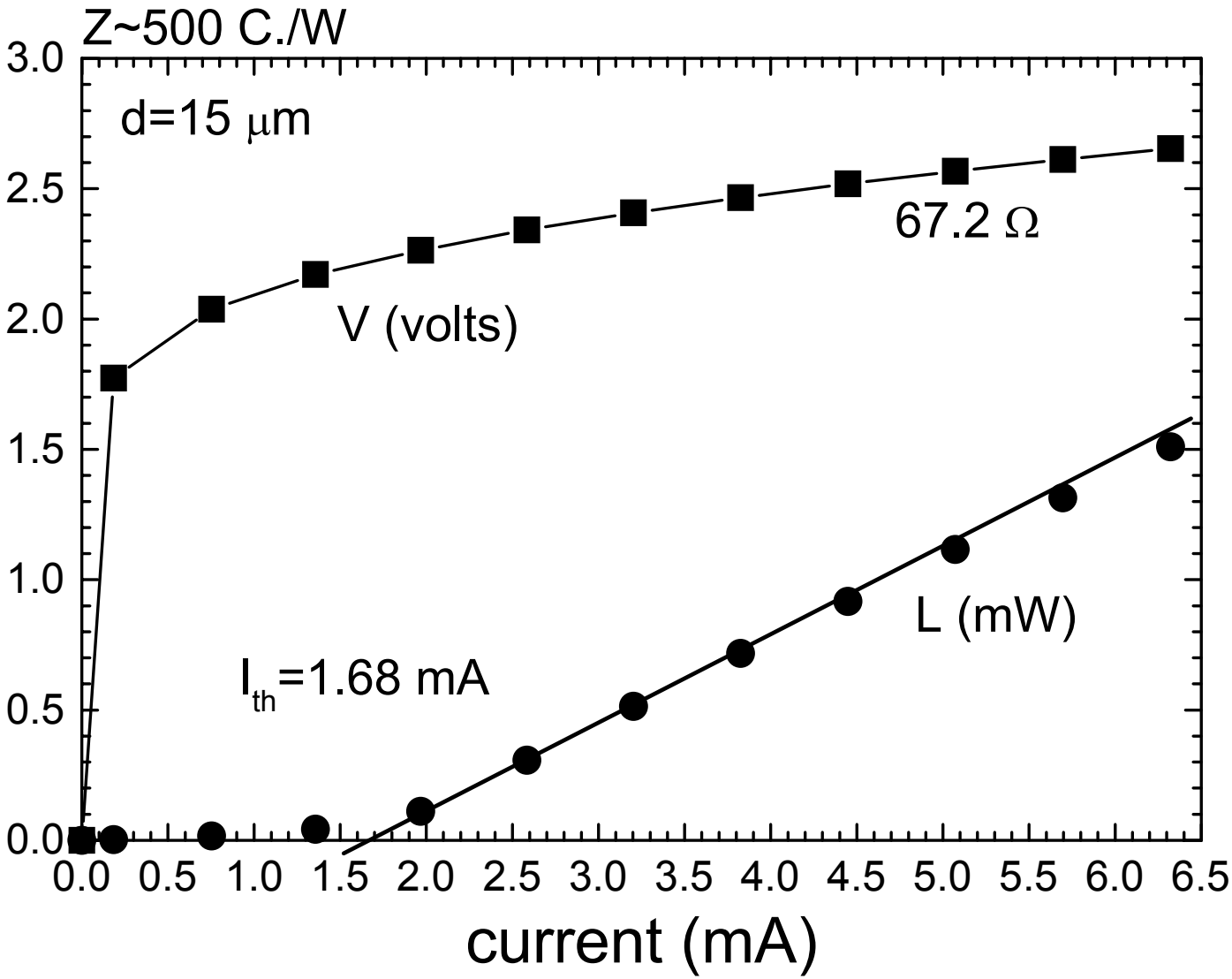
Lower thermal impedance can be achieved if flip-chip bump is used to convey heat



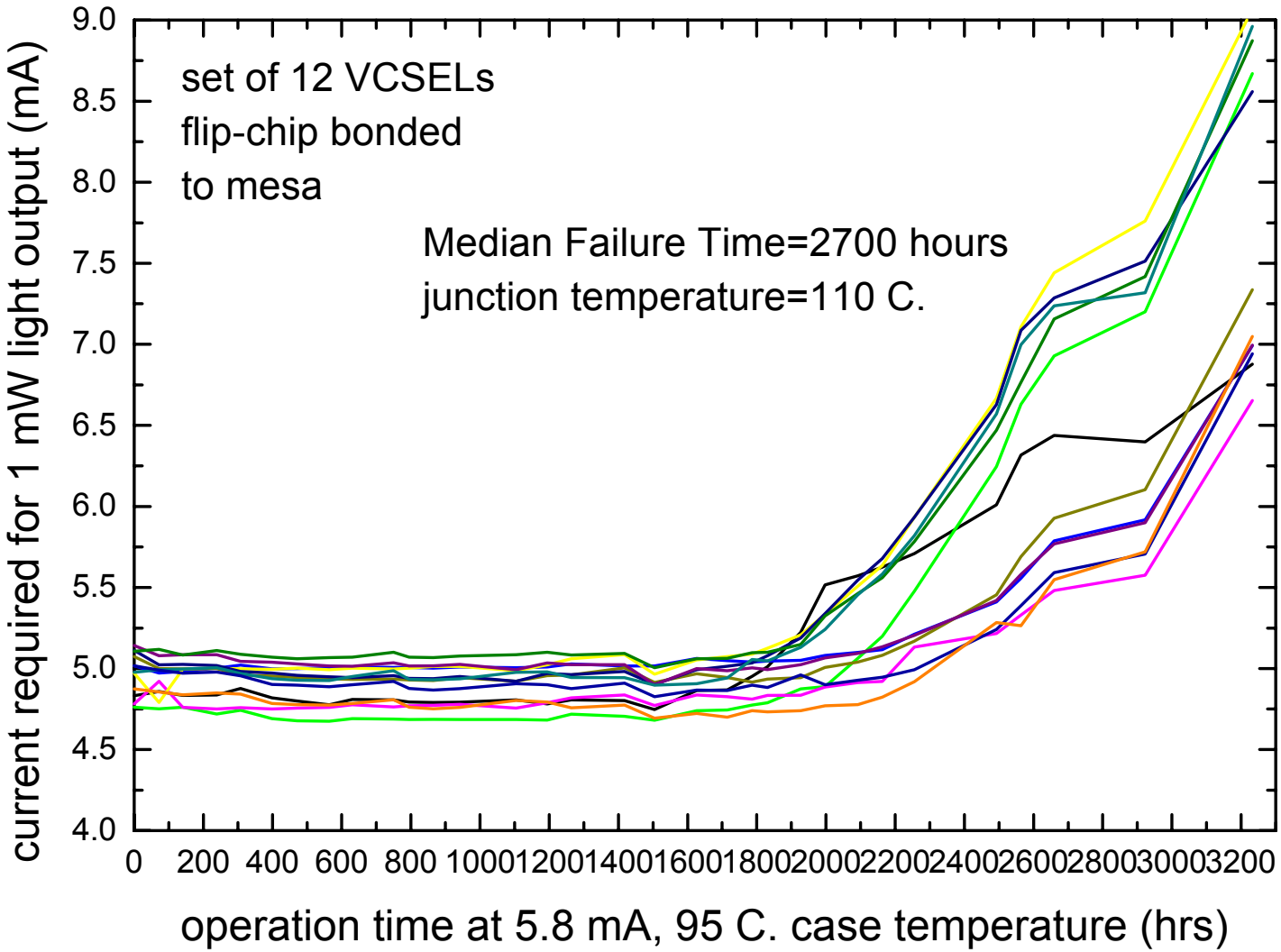
Even direct bonding results in high thermal impedance, due to Bragg mirror, which can be reduced by adding gold layer



Using this technique, we have achieved about 500 C./W thermal impedance



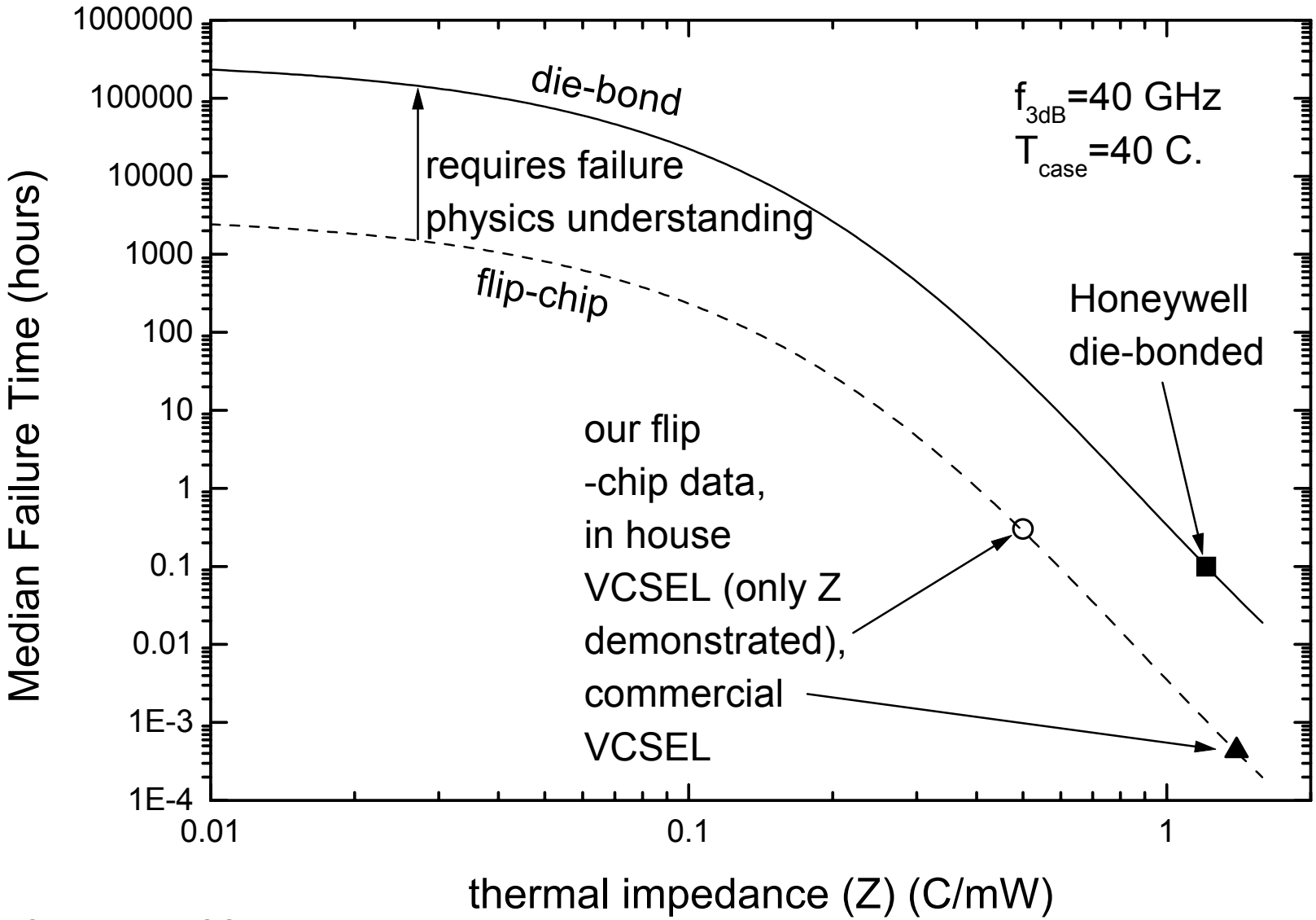
However, bonding directly to the mesa, while lowering junction temperature, causes ~ 96 times faster failure at a given junction temperature and current (A=12.5)



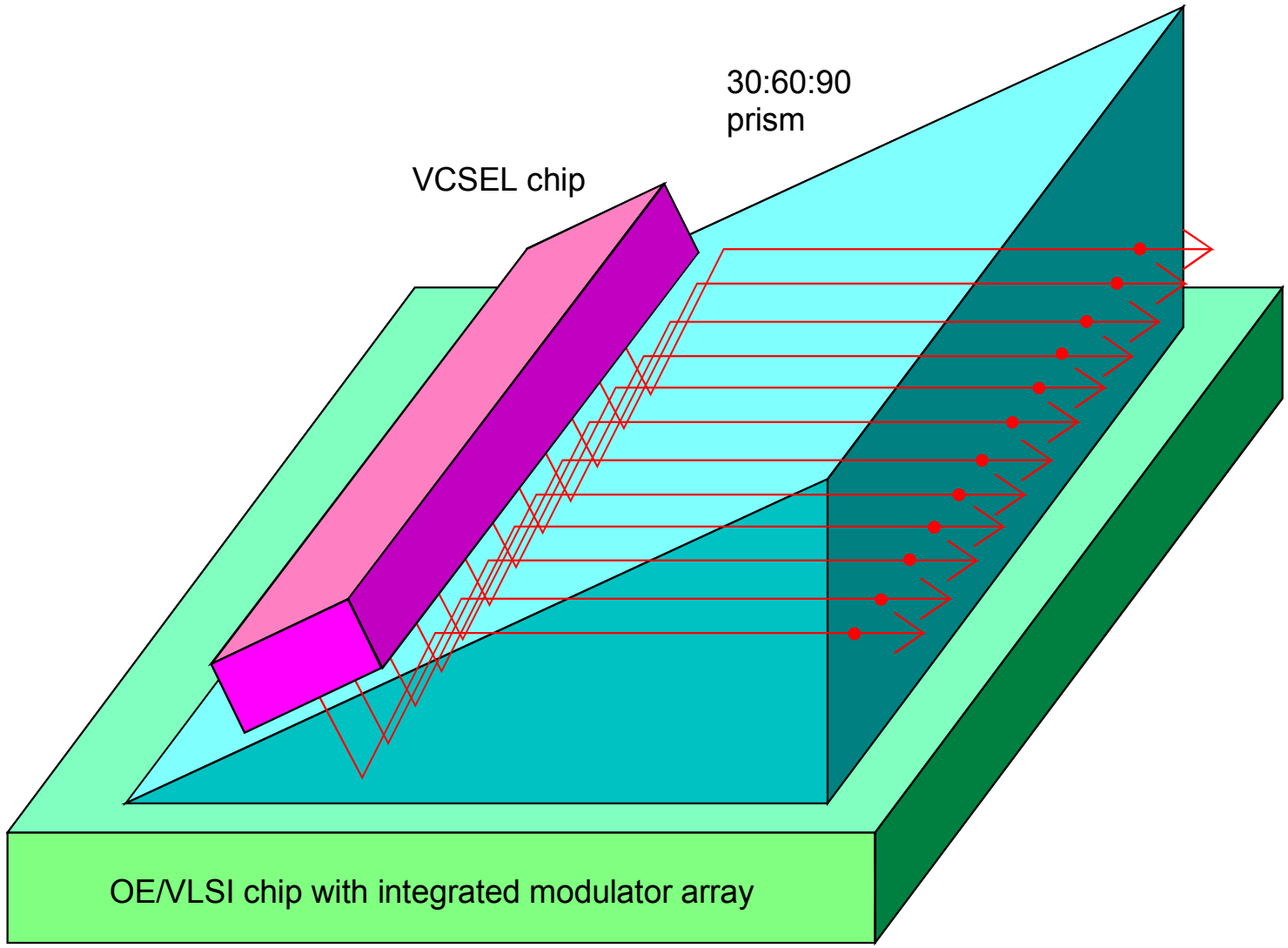
The VCSEL thermal quandary

Making the VCSEL run cooler requires intimate placement of heat sinking bonds to the active region, but that increases failure rate at a given temperature!

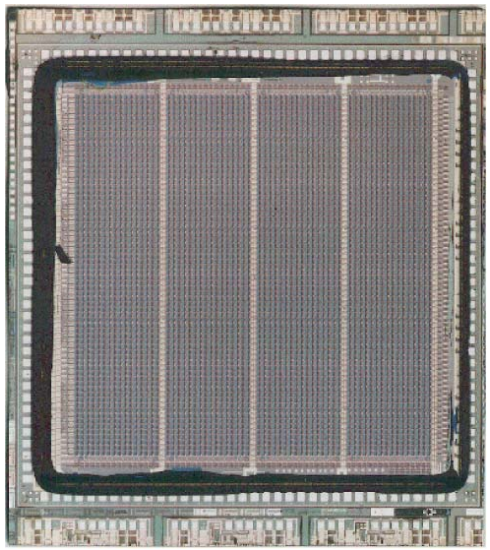
Thermal impedance requirements for 40 Gbit/sec

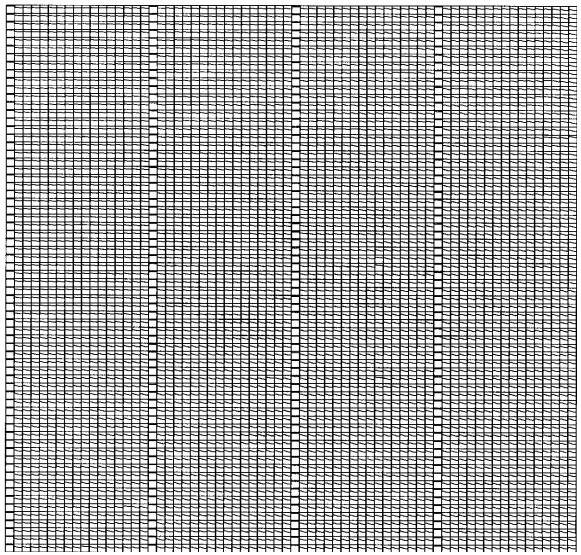


Proposed 1x12 modulator transmit module with on-board VCSEL readout lasers



Modulators vs. VCSEL's

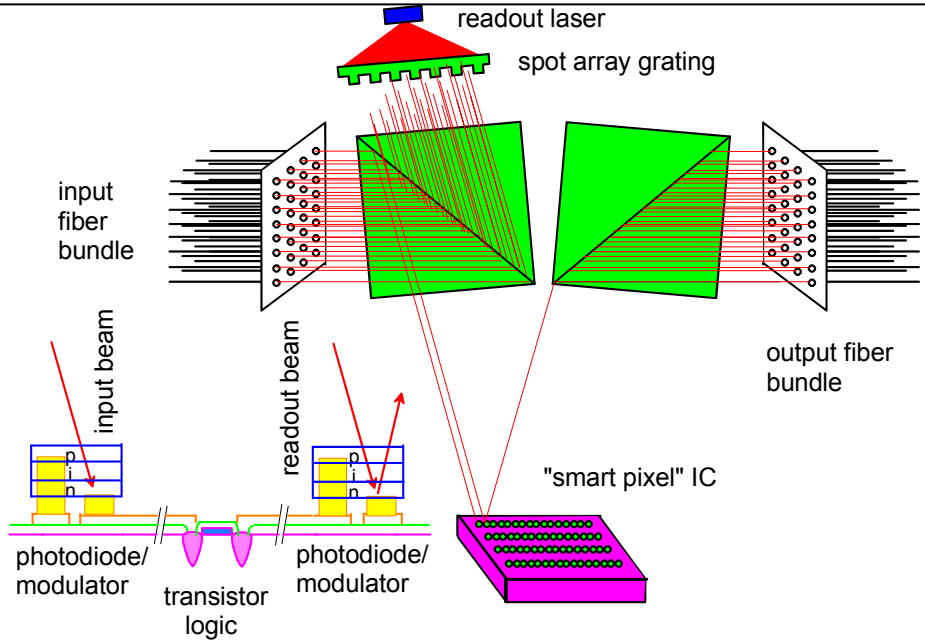


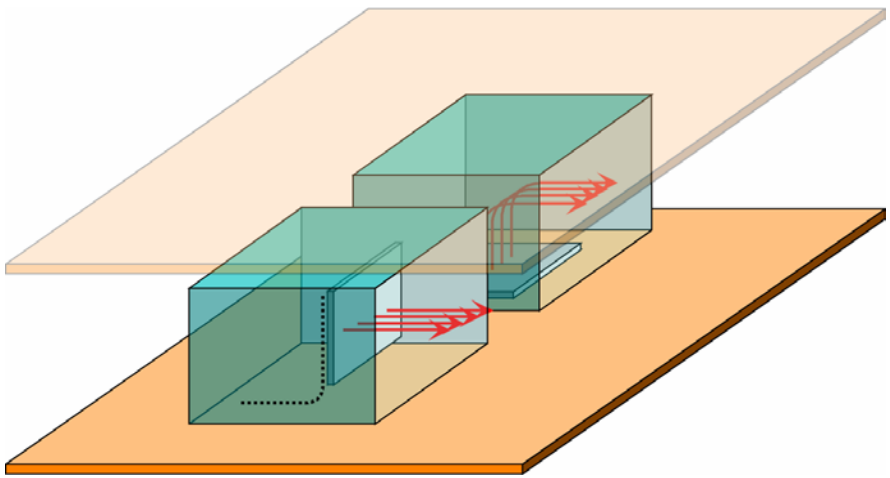


Modulators: chips can be made with thousands all working (Bell Labs).

VCSEL's: chips can be made with tens all working (Aralight).

Modulators vs. VCSEL's





Modulators: packaging (nightmare ?).

VCSEL's: essentially butt-coupled; relatively well developed.

Technology observations

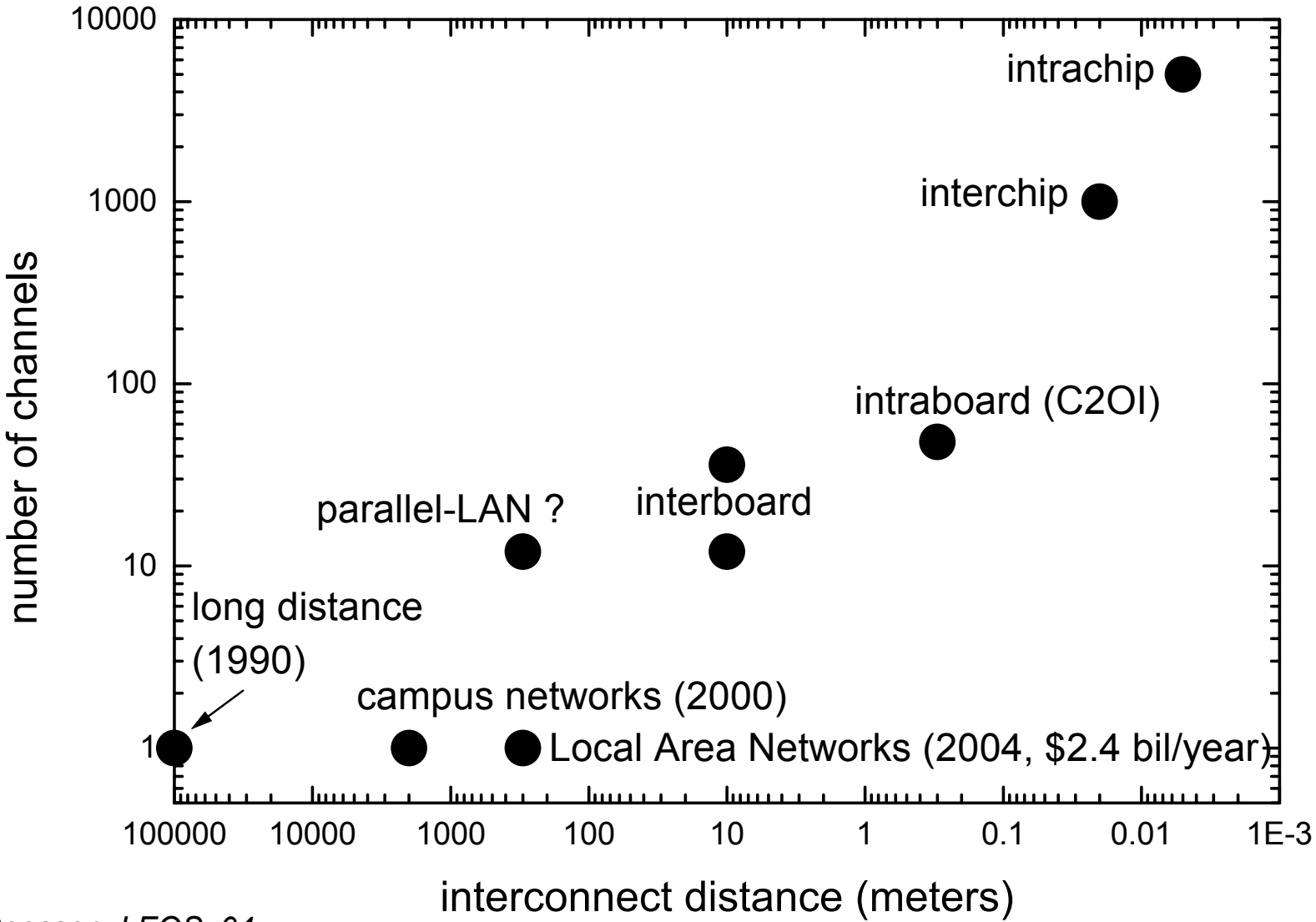
● Early system experiments into the use of optical interconnects ignored third dimension (rack) physical constraints and assumed an open structure.

● Fitting (surface normal, e.g. VCSEL) optical interconnects to a rack structure requires bending either the light or electrical drive through a 90^{o} turn- most workers in the field agree that it is easier to do the latter via a flexible board.

● Packaging of linear VCSEL arrays is facilitated by optically accurate ferrule mating pins fixed to the board; however, 2D (flip-chip) arrays suffer from the driver chip being in the way. Can we just etch pin access holes through it?

● Curve fitting Honeywell reliability data results in very effective model that predicts lifetime limit of VCSEL systems to ~ 20 Gbit/sec channel rate. Reducing thermal impedance to zero alleviates this, but may not be practical. Do we need external modulators?

What is the future path of optical interconnects?



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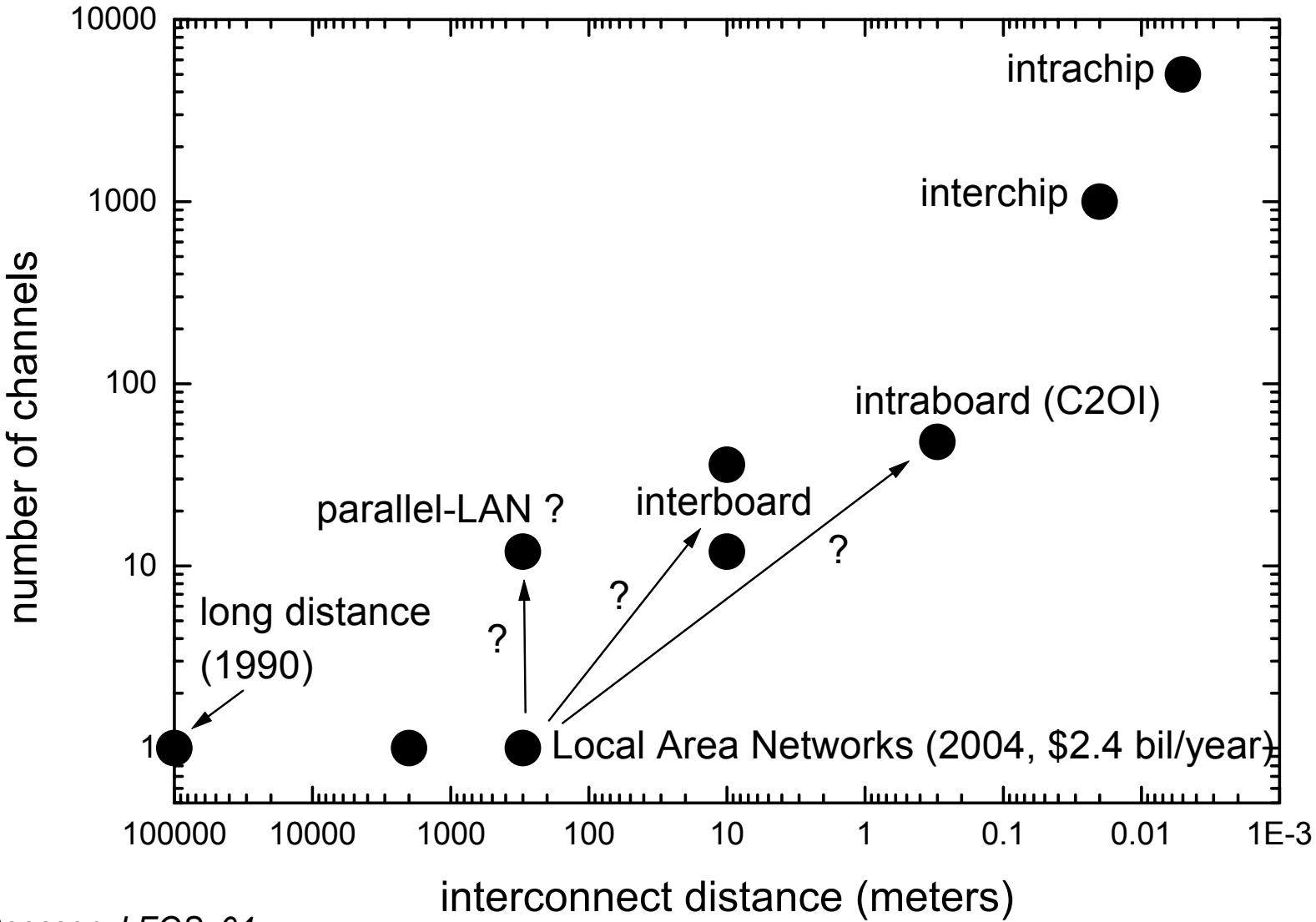

Conclusion

● An evolutionary path to optical interconnects would employ denser and denser modules, respecting the rack system paradigm.

● Allowing advanced packaging such as water cooling, such a 1000 channel module could be constructed and would be ~ 30x30 mm.

● Only an extremely compelling performance/cost argument would allow shifting away from the rack paradigm to allow full utilization of the third dimension for optical interconnects.