

Contents

Volume 1

Introduction

Introduction	1–1
The Verilog Hardware Description Language	1–1
The Verilog–XL Logic Simulator	1–3
Major Features of Verilog–XL	1–3
Verilog–XL Licenses	1–4

Lexical Conventions

Lexical Conventions	2–1
Operators	2–1
White Space and Comments	2–2
Numbers	2–2
Strings	2–5
String Variable Declaration	2–5
String Manipulation	2–6
Special Characters in Strings	2–7
Identifiers, Keywords, and System Names	2–7
Escaped Identifiers	2–8
Keywords	2–9
Text Substitutions	2–9

Data Types

Data Types	3–1
Value Set	3–1
Registers and Nets	3–2

Return to MAIN MENU

Registers	3-2
Declaration Syntax	3-3
Declaration Examples	3-4
Vectors	3-5
Specifying Vectors	3-5
Vector Net Accessibility	3-5
Strengths	3-6
Charge Strength	3-6
Drive Strength	3-7
Implicit Declarations	3-7
Net Initialization	3-7
Net Types	3-8
wire and tri Nets	3-8
Wired Nets	3-8
triereg Net	3-9
tri0 and tri1 Nets	3-13
supply Nets	3-13
Memories	3-14
Integers and Times	3-16
Real Numbers	3-17
Declaration Syntax for Real Numbers	3-17
Specifying Real Numbers	3-17
Operators and Real Numbers	3-18
Conversion	3-18
Parameters	3-19

Expressions

Expressions	4-1
Operators	4-2
Binary Operator Precedence	4-4
Numeric Conventions in Expressions	4-5
Arithmetic Operators	4-5
Arithmetic Expressions with Registers and Integers ..	4-6
Relational Operators	4-7

Equality Operators	4-8
Logical Operators	4-9
Bit-Wise Operators	4-11
Reduction Operators	4-12
Syntax Restrictions	4-14
Shift Operators	4-15
Conditional Operator	4-15
Concatenations	4-16
Operands	4-17
Net and Register Bit Addressing	4-17
Memory Addressing	4-18
Strings	4-19
String Operations	4-20
String Value Padding and Potential Problems ..	4-20
Null String Handling	4-22
Minimum, Typical, Maximum Delay Expressions ..	4-22
Expression Bit Lengths	4-23
An Example of an Expression Bit Length Problem ...	4-24
Verilog Rules for Expression Bit Lengths	4-24

Assignments

Assignments	5-1
Continuous Assignments	5-2
The Net Declaration Assignment	5-3
The Continuous Assignment Statement	5-3
Delays	5-5
Strength	5-9
Procedural Assignments	5-9
Accelerated Continuous Assignments	5-10
The Restrictions on Accelerated	
Continuous Assignments	5-10
How to Control the Acceleration of	
Continuous Assignments	5-22
The Effects of Accelerated Continuous Assignments	5-24

Gate and Switch Level Modeling

Gate and Switch Level Modeling 6-1

Gate and Switch Declaration Syntax 6-2

and, nand, nor, or, xor, and xnor Gates 6-6

buf and not Gates 6-8

bufif1, bufif0, notif1, and notif0 Gates 6-9

MOS Switches 6-10

Bidirectional Pass Switches 6-12

cmos Gates 6-13

pullup and pulldown Sources 6-14

Implicit Net Declarations 6-15

Logic Strength Modeling 6-16

Strengths and Values of Combined Signals 6-18

 Combined Signals of Unambiguous Strength ... 6-18

 Ambiguous Strengths: Sources and Combinations 6-20

 Ambiguous Strength Signals and
 Unambiguous Signals 6-26

 Wired Logic Net Types 6-30

Mnemonic Format 6-33

Strength Reduction by Non-Resistive Devices 6-33

Strength Reduction by Resistive Devices 6-33

Strengths of Net Types 6-34

 tri0 and tri1 Net Strengths 6-34

 trireg Strength 6-34

 supply0 and supply1 Net Strengths 6-34

Gate and Net Delays 6-34

 min/typ/max Delays 6-37

 trireg Net Charge Decay 6-39

Gate and Net Name Removal 6-43

User-Defined Primitives (UDPs)

De

User-Defined Primitives (UDPs) 7-1

Memory Usage and Performance Considerations 7-2

Syntax 7-3

UDP Definition	7-4
UDP Terminals	7-5
UDP Declarations	7-5
Sequential UDP initial Statement	7-5
UDP State Table	7-5
Combinational UDPs	7-6
Level-Sensitive Sequential UDPs	7-8
Edge-Sensitive UDPs	7-9
Sequential UDP Initialization	7-10
UDP Instances	7-14
Compilation	7-14
Symbols to Enhance Readability	7-15
Mixing Level-Sensitive and Edge-Sensitive Descriptions	7-16
Reducing Pessimism	7-17
Level-Sensitive Dominance	7-19
Processing of Simultaneous Input Changes	7-19
Summary of Symbols	7-21
Examples	7-22

Behavioral Modeling

Behavioral Modeling	8-1
Behavioral Model Overview	8-1
Procedural Assignments	8-3
Blocking Procedural Assignments	8-4
The Non-Blocking Procedural Assignment	8-4
How the Simulator Processes Blocking and Non-Blocking Procedural Assignments	8-11
Conditional Statement	8-11
if-else-if Construct	8-14
Example	8-15
Case Statement	8-16
Case Statement with Don't-Cares	8-19
Looping Statements	8-20
forever Loop	8-21
repeat Loop Example	8-22

while Loop Example	8-23
for Loop Examples	8-23
Procedural Timing Controls	8-25
Delay Control	8-26
Zero-Delay control	8-26
Event Control	8-27
Named Events	8-28
Event OR Construct	8-29
Level-Sensitive Event Control	8-29
Intra-Assignment Timing Controls	8-30
Block Statements	8-35
Sequential Blocks	8-35
Parallel Blocks	8-37
Block Names	8-39
Start and Finish Times	8-39
Structured Procedures	8-41
initial Statement	8-42
always Statement	8-43
Examples	8-43

Tasks and Functions

Tasks and Functions	9-1
Distinctions Between Tasks and Functions	9-1
Tasks and Task Enabling	9-2
Defining a Task	9-3
Task Enabling and Argument Passing	9-4
Task Example	9-6
Effect of Enabling an Already Active Task	9-7
Functions and Function Calling	9-8
Defining a Function	9-8
Returning a Value from a Function	9-9
Calling a Function	9-9
Function Rules	9-10
Function Example	9-11