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Modelling and Analysis of Computer Network Clocks

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Abstract

This report describes analytical models and design methodologies for computer clocks synchronized to other clocks in a computer network or internetwork. This requires each clock to function as a disciplined oscillator which can be adjusted in both time and frequency to compensate for the intrinsic errors of the onboard frequency source. It also requires the use of a time-synchronization protocol such as the Network Time Protocol, summarized briefly in this report, or the Digital Time Synchronization Service, described elsewhere.

The goal in this effort is to improve the synchronization accuracy from the tens of milliseconds regime of present timekeeping models to the submillisecond regime. In this report analytical models are used to express the accuracy and stability of a computer clock and to establish its design parameters with respect to time and frequency error tolerances. These models are based on the theory of adaptive-parameter, phase-lock loops. Included is a discussion on methods to combine the timing information received from a number of synchronized peer clocks to improve the accuracy and reliability of the local clock. Finally, a detailed analysis of the maximum and expected errors accumulated from the primary source of time throughout the synchronization subnet is presented.

Keywords: clock modelling, computer clock, synchronization error analysis, disciplined oscillator, synchronization algorithms, time synchronization, network synchronization.

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