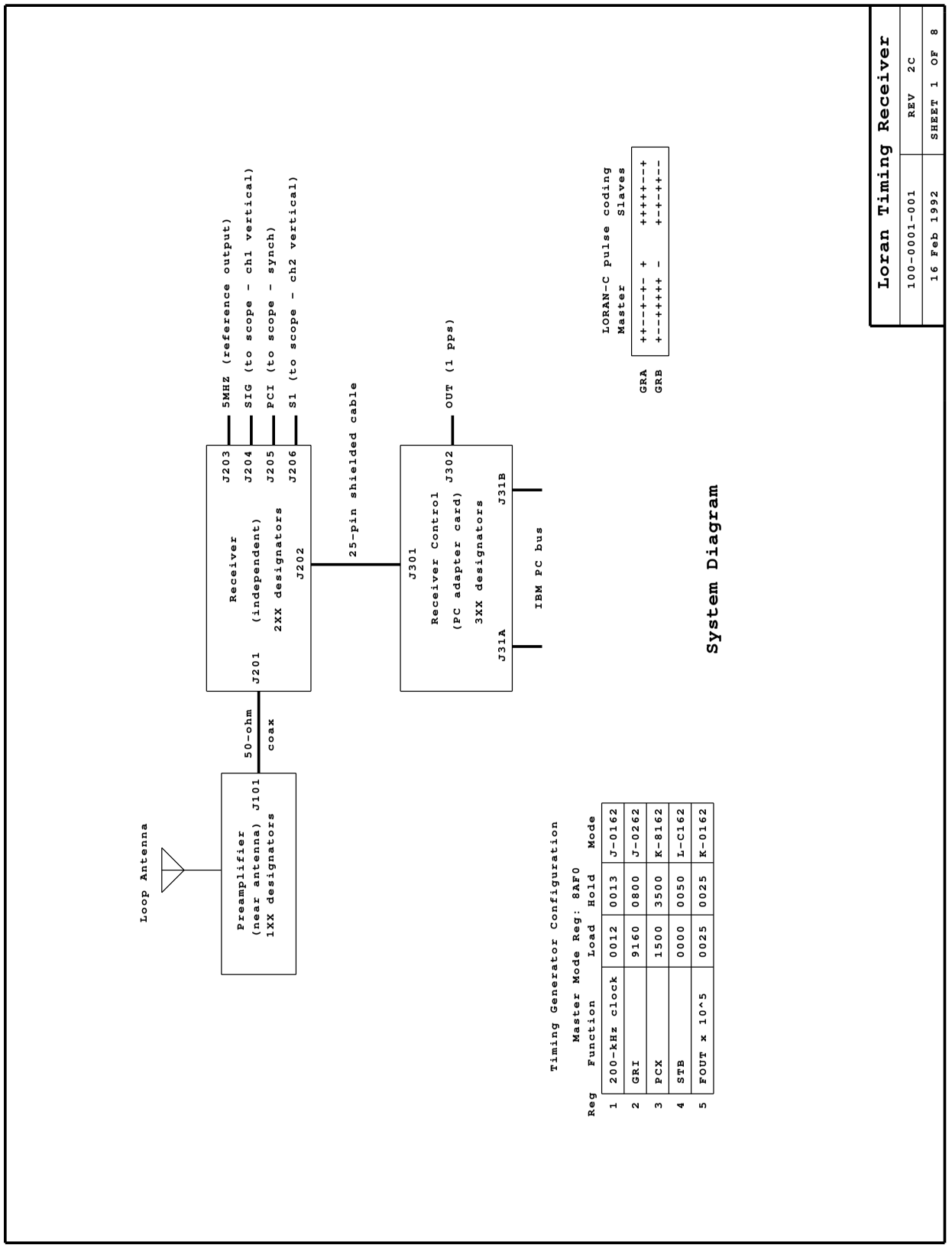
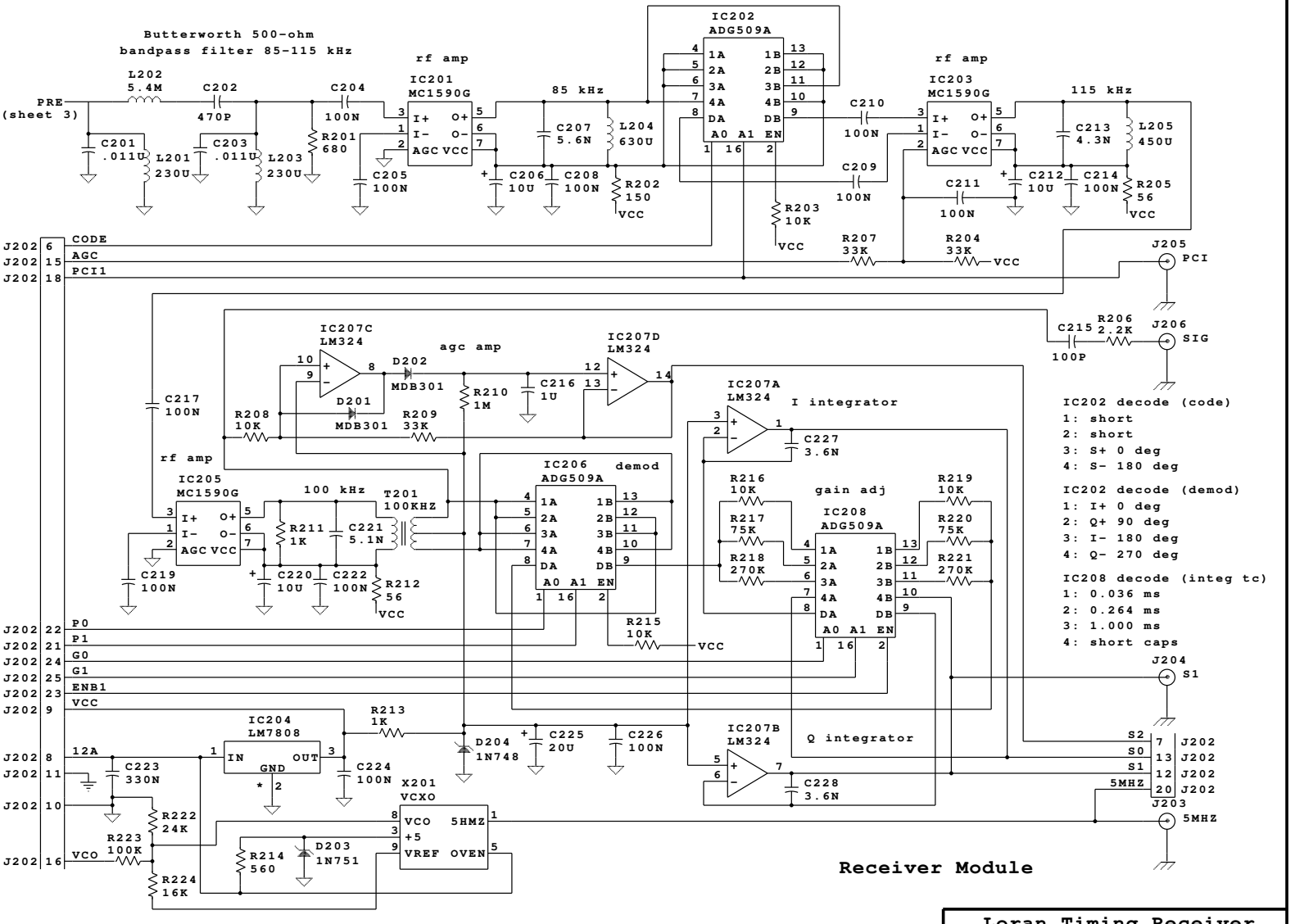
Appendix C. Schematic Drawings



Reg	Function	Load	Hold	Mode
1	200-kHz clock	0012	0013	J-0162
2	GRI	9160	0800	J-0262
3	PCX	1500	3500	K-8162
4	STB	0000	0050	L-C162
5	FOUT x 10^5	0025	0025	K-0162


Butterworth 500-ohm
bandpass filter 85-115 kHz
rf amp
IC201
MC1590G
85 kHz
IC202
ADG509A
rf amp
IC203
MC1590G
115 kHz
PRE
(sheet 3)
L202
5.4M
C202
470P
C204
100N
C201
.011U
L201
230U
C203
.011U
L203
230U
R201
680
C205
100N
C206
10U
C207
5.6N
C208
100N
L204
630U
R202
150
VCC
R203
10K
C210
100N
C209
100N
C211
100N
C212
10U
C213
4.3N
C214
100N
L205
450U
R205
56
R207
33K
R204
33K
J205
PCI
J206
SIG
C215
100P
R206
2.2K
J202 6 CODE
J202 15 AGC
J202 18 PCI1
IC207C
LM324
agc amp
IC207D
LM324
D202
MDB301
D201
MDB301
R208
10K
R209
33K
R210
1M
C216
1U
C217
100N
IC207A
LM324
I integrator
C227
3.6N
rf amp
IC205
MC1590G
100 kHz
T201
100KHZ
R211
1K
C221
5.1N
C219
100N
C220
10U
C222
100N
R212
56
IC206
ADG509A
demod
R216
10K
R217
75K
R218
270K
IC208
ADG509A
gain adj
R219
10K
R220
75K
R221
270K
R215
10K
J202 22 P0
J202 21 P1
J202 24 G0
J202 25 G1
J202 23 ENB1
J202 9 VCC
IC204
LM7808
R213
1K
D204
1N748
C225
20U
C226
100N
IC207B
LM324
Q integrator
C228
3.6N
J202 8 12A
J202 11
J202 10
J202 16 VCO
C223
330N
C224
100N
X201
VCXO
R222
24K
R223
100K
R224
16K
R214
560
D203
1N751
5MHZ
J203
5MHZ
J204
S1
S2
S0
S1
J202
IC202 decode (code)
1: short
2: short
3: S+ 0 deg
4: S- 180 deg
IC202 decode (demod)
1: I+ 0 deg
2: Q+ 90 deg
3: I- 180 deg
4: Q- 270 deg
IC208 decode (integ tc)
1: 0.036 ms
2: 0.264 ms
3: 1.000 ms
4: short caps
Receiver Module
* note: connect digital and analog grounds together at IC204 pin 2
T1: 100-kHz transformer 3 windings each 500U
14x3 turns #28 Amidon FT50/75 ferrite
Loran Timing Receiver
100-0001-001
REV 2C
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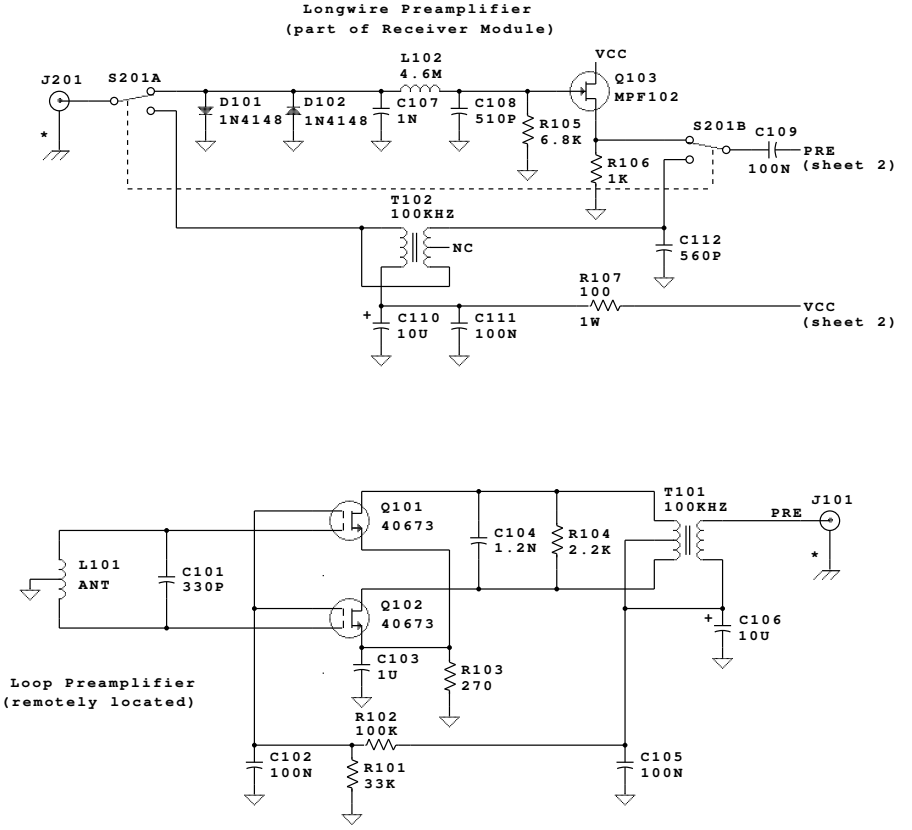

Preamplifier Modules

L101: 100-kHz loop antenna 12.5M
50x2 turns #28 24" diameter shielded

T101, T102: 100-kHz transformer 3 windings 500U each
14x3 turns #28 Amidon FT50/75 ferrite

* note: connect analog and chassis grounds
together at J101 and J201 shields

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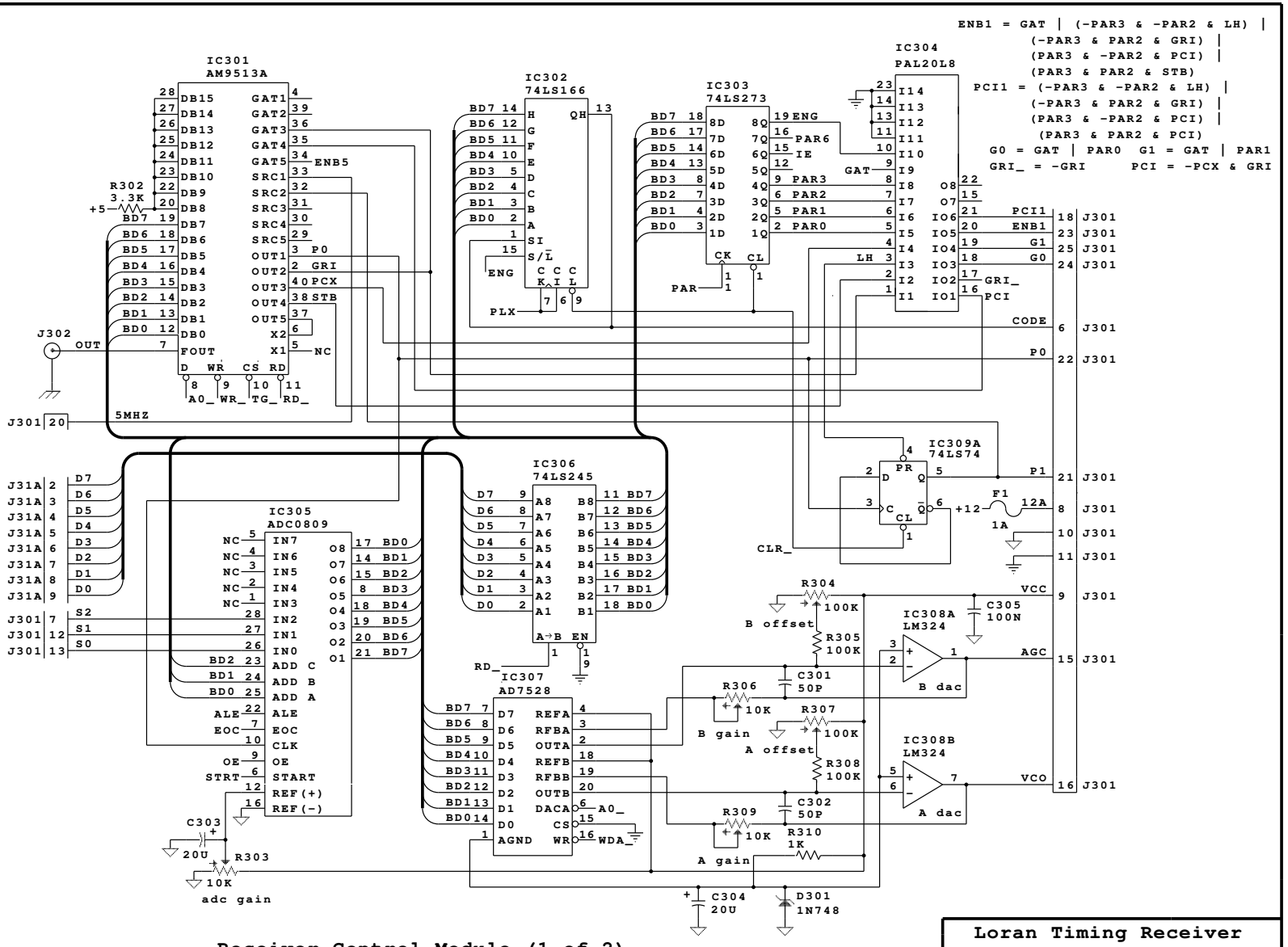
ENB1 = GAT | (-PAR3 & -PAR2 & LH) |
(-PAR3 & PAR2 & GRI) |
(PAR3 & -PAR2 & PCI) |
(PAR3 & PAR2 & STB)
PCI1 = (-PAR3 & -PAR2 & LH) |
(-PAR3 & PAR2 & GRI) |
(PAR3 & -PAR2 & PCI) |
(PAR3 & PAR2 & PCI)
G0 = GAT | PAR0 G1 = GAT | PAR1
GRI_ = -GRI PCI = -PCX & GRI
IC301
AM9513A
IC302
74LS166
IC303
74LS273
IC304
PAL20L8
IC305
ADC0809
IC306
74LS245
IC307
AD7528
IC308A
LM324
IC308B
LM324
IC309A
74LS74
R302
3.3K
R303
10K
adc gain
R304
100K
B offset
R305
100K
R306
10K
B gain
R307
100K
A offset
R308
100K
R309
10K
A gain
R310
1K
C301
50P
C302
50P
C303
20U
C304
20U
C305
100N
D301
1N748
F1
12A
1A
J302
OUT
5MHZ
B dac
A dac
AGC
VCO
CODE
P0
P1
CLR_
RD_
PLX
PAR
Receiver Control Module (1 of 2)
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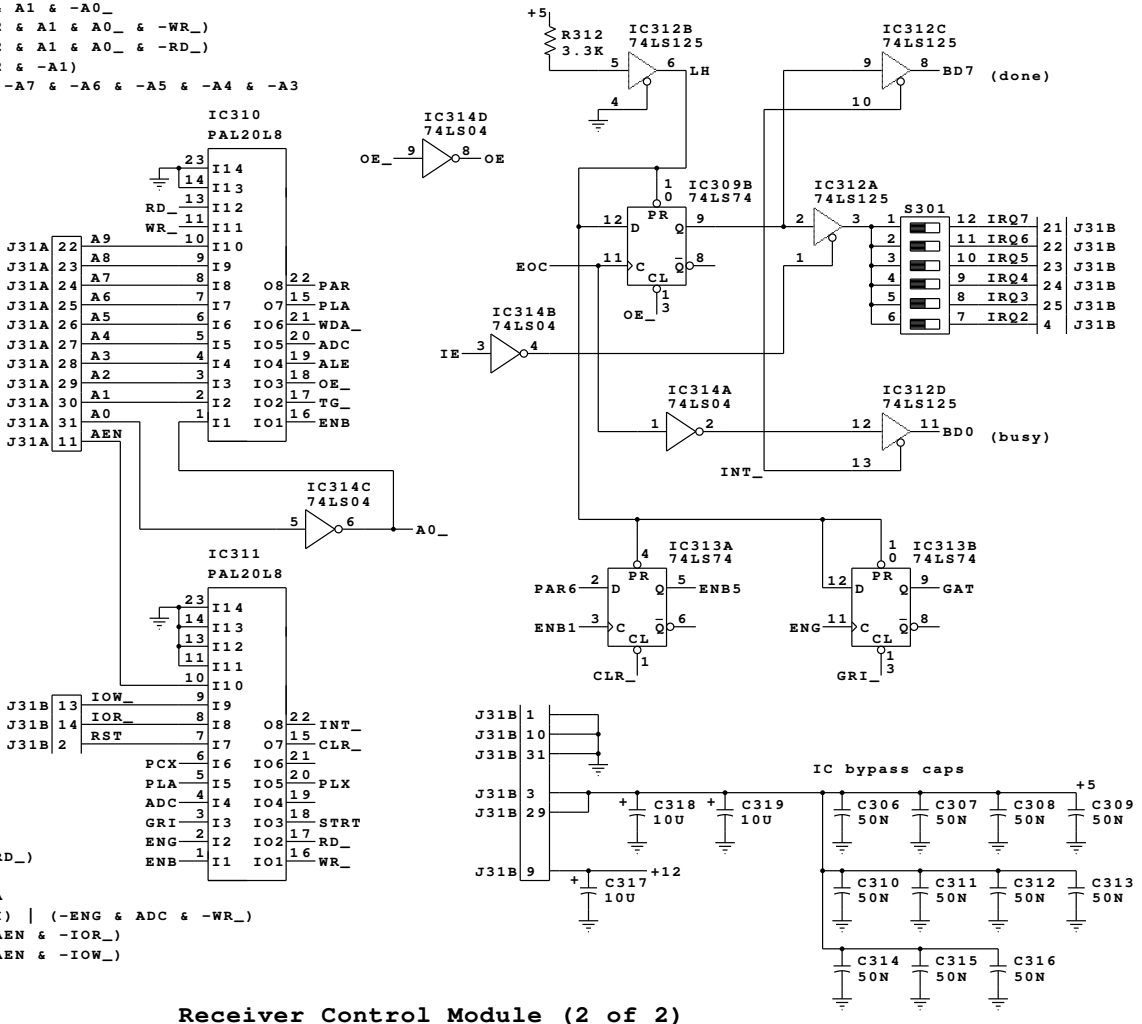
```
111W PAR  = -(A2 & A1 & -A0_ & -WR_)
110W PLA  = -(A2 & A1 & A0_ & -WR_)
10XW WDA_ = -(A2 & -A1 & -WR_)
011X ADC  = -A2 & A1 & -A0_
010W ALE  = -(-A2 & A1 & A0_ & -WR_)
010R OE_  = -(-A2 & A1 & A0_ & -RD_)
00XX TG_  = -(-A2 & -A1)
ENB  = A9 & A8 & -A7 & -A6 & -A5 & -A4 & -A3
```




```
INT_ = -(ADC & -RD_)
CLR_ = -RST
PLX  = -PCX & PLA
STRT = (ENG & GRI) | (-ENG & ADC & -WR_)
RD_  = -(ENB & -AEN & -IOR_)
WR_  = -(ENB & -AEN & -IOW_)
```

Receiver Control Module (2 of 2)

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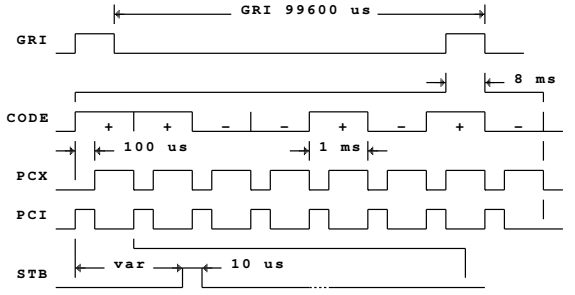

Figure 1. Gating Signals

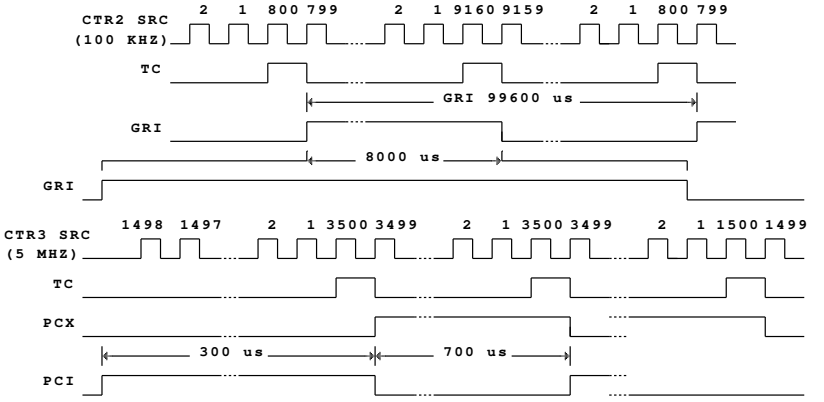

Figure 2. Timing Generator

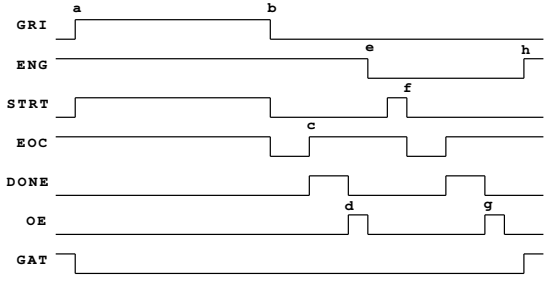

Figure 3. System Operation

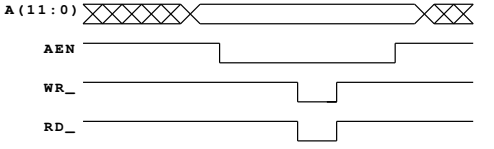

Figure 4. Computer Bus Interface Sequencing

Timing Diagrams

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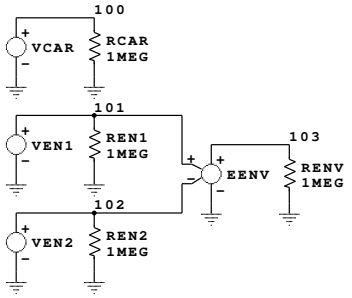
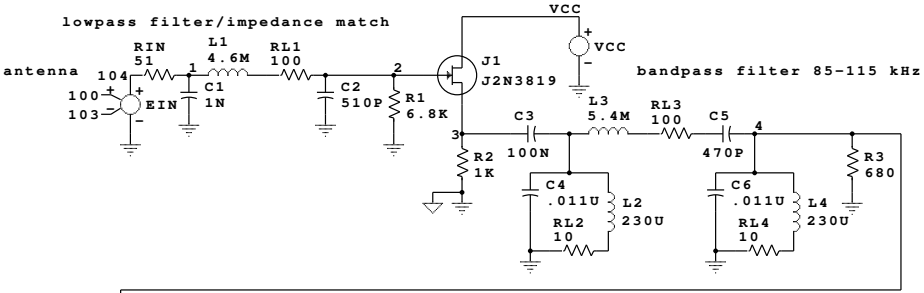
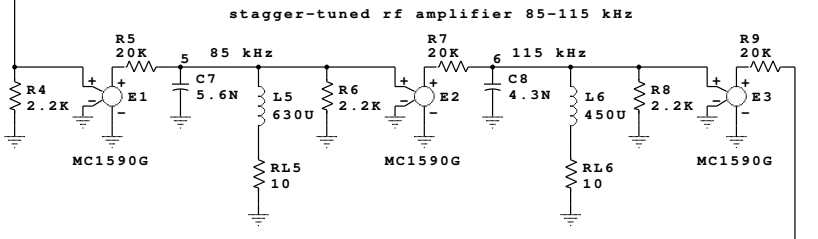
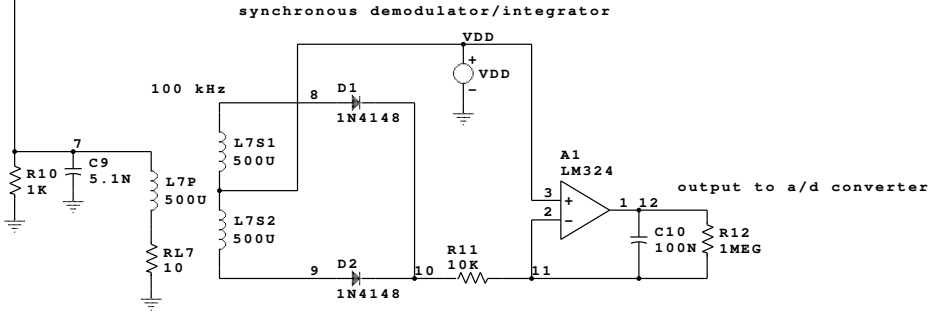


LORAN-C waveform generator








```
.1      .TRAN 1U 500U
.2      .PRINT TRAN V(1) V(8) V(9)
.3      * .TF V(8) VIN
.4      * .AC DEC 200 30K 300K
.5      .PRINT AC VCB(8) VDB(6) VDB(5) VDB(4) VDB(1)
.6      .PROBE
.7      .LIB EVAL.LIB
 X1     VDD 11 VCC 0 12 LM324
 K1      L7P L7S1 L7S2 0.9
```

PSPICE Simulation – Rf Circuits

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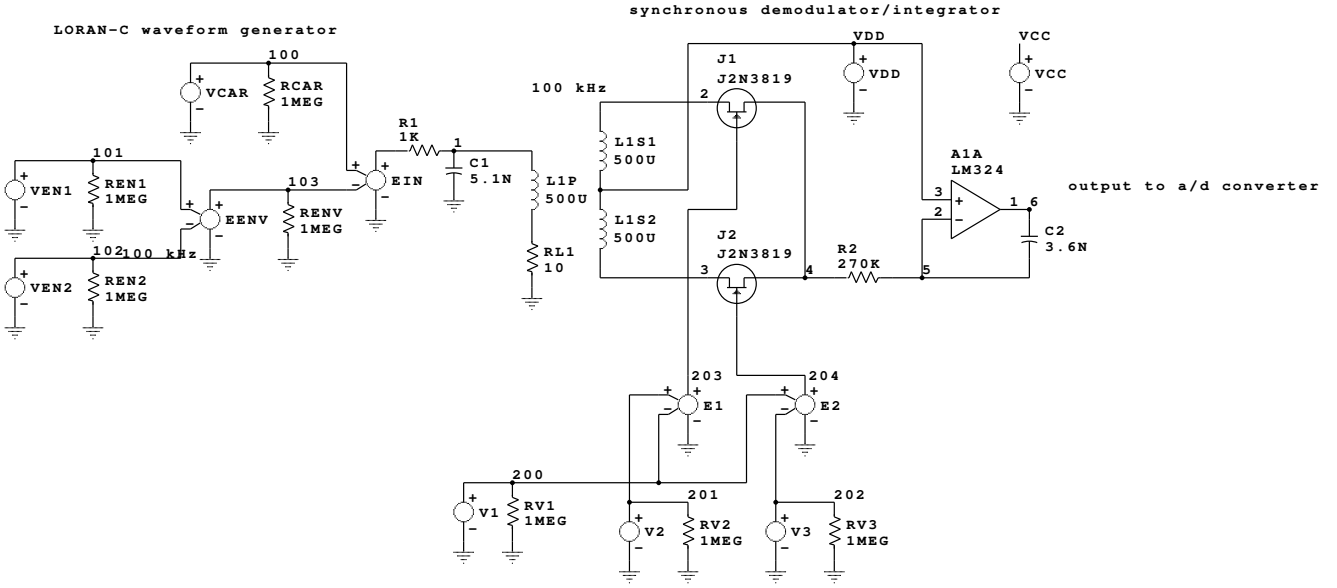


```
.1      .TRAN 1U 500U
.2      .OPTION ITL5=0
.3      .IC V(4)=4
.4      .PRINT TRAN V(1) V(6)
.5      * .TF V(8) VIN
.6      * .AC DEC 200 30K 300K
.7      * .PRINT AC VDB(1)
.8      .PROBE
.9      .LIB EVAL.LIB
 X1     VDD 5 VCC 0 6 LM324
 X2     7 3 VCC 0 8 LM324
 X3     VDD 5 VCC 0 6 LM324
 K1      L1P L1S1 L1S2 0.95
```

PSPICE Simulation – Demod and Integrator Circuits

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