Appendix A. Host Computer Interface

The host computer interface is contained on a plug-in module designed for the IBM PC/XT/AT bus. It includes the converters, counters, registers and programmed-logic components which control the receiver and produce timing signals. It normally produces an interrupt upon completion of each A/D conversion, which occurs three times in each GRI (one each for the I and Q integrators, plus a third for the signal-level indicator), which results in between 30 and 75 interrupts per second, depending on the LORAN-C chain rate or GRI. At interrupt time the program can modify the timing generator registers, read the A/D converter buffer (ADCBUF), set the A/D converter multiplexor address (ADCMUX), pulse-code buffer (PCBUF) and parameter register (PAR) for the next GRI. Since the integrators used in the receiver itself accumulate only over the 8-ms PCI, it is the responsibility of the program to accumulate these three channels of data for subsequent GRIs. At any time the program can output previously computed values to the D/A converter A (DACA) and D/A converter B (DACB) to set the precision oscillator frequency and receiver gain control voltages, respectively.

A.1. Programming Registers

The receiver has eight programming registers located in the port block 0300-0307 (hex) as shown in Figure A.13 and described below.

A.1.1. 0300 AMD9513A Timing Generator (control) (TGC) and 0301 AMD9513A Timing Generator (data) (TGD)

The TGC and TGD registers correspond to the control and data paths described in the AMD9513A documentation. Both registers are read/write.

A.1.2. 0302 A/D Converter Buffer and Multiplexor Address (ADCBUF)

For read operations the ADCBUF register contains the result of the most recent A/D conversion. The data are accurate for only a few milliseconds, since the integrators have a small but significant amount of leakage. The data format is offset-binary, with 0 the most negative value, 255 the most positive and 128 the nominal zero value. When the data are read, bit 7 (DONE) of the ADCGO register is automatically cleared.

0300	TGC	Timing Generator Control (read/write)
0301	TGD	Timing Generator Data (read/write)
0302	ADCBUF	ADC Buffer (read) ADC Multiplexor Address (write)
0303	ADCGO	ADC Status (read) ADC Start (write)
0304	DACA	DAC A (VCO) Buffer (write)
0305	DACB	DAC B (AGC) Buffer (write)
0306	CODE	Pulse Code Buffer (write)
0307	PAR	Parameter Buffer (write)

Figure A.1. Receiver Controller Registers

For write operations the ADCBUF register contains the multiplexor address for the input to be converted. Note that an A/D conversion cannot be started until 50 ns after the multiplexor address has settled; therefore, the two operations cannot be combined in the same instruction. The multiplexor address assignments are given in the following table:

Channel	Input
0	I channel integrator output (1-7 V)
1	Q channel integrator output (1-7 V)
2	receiver signal level (1-7 V)
3-7	not used

A.1.3. 0303 A/D Converter Status and A/D Converter Start (ADCGO)

For read operations bit 0 (BUSY) indicates the A/D converter is actively converting a value, while bit 7 (DONE) indicates the conversion has completed and data are ready to be read from the ADCBUF register. For write operations the ADCGO register is used to start an A/D conversion, which normally takes about 100 μs. Writing anything to this register starts the conversion and sets bit 0 (BUSY) of the ADCGO register. When complete, bit 0 is cleared, bit 7 (DONE) is set and an interrupt is signalled at the PC interrupt level determined by dipswitch S301 (see Drawing Sheet 5).

A.1.4. 0304 D/A Converter A (DACA) and 0305 D/A Converter B (DACB)

The DACA and DACB registers contain the values to be converted to analog representation and are write-only. The data format is offset-binary, with 0 the most negative value, 255 the most positive and 128 the nominal zero value. DACA controls the gain of the receiver, while DACB controls the precision oscillator frequency. The gain and offset for each DAC can be adjusted by potentiometers as specified in the following table:

DAC	Function	Offset	Gain
A	osc frequency	R307	R309
B	receiver gain	R304	R306

A.1.5. 0306 Pulse-Code Buffer (CODE)

The PCBUF register contains the LORAN-C pulse phase code for the selected master or slave station and is write-only. The pulses are transmitted beginning with the most significant (leftmost) bit with a value of 0 corresponding to a "-" code and 1 corresponding to a "+" code.

A.1.6. 0307 Parameter Buffer (PAR)

The PAR register is used to control various details of system operation. The bits of the 8-bit byte are interpreted according to the following figure. (The unlabeled bits are not used.)

7	6	5	4	3	2	1	0
ENG				GATE1	GATE0	TC1	TC0

If bit 7 (ENG) is set, the A/D converter starts automatically at the end of the next GRI; if clear, the converter is started by the program upon a write to the ADCGO register. Bits GATE[1:0] select the gating source for the rf and integrator switches according to the following table.

GATE[1:0]	rf switch	integ switch
0	always on	always on
1	GRI	GRI
2	PCI	PCI
3	PCI	STB

Bits TC[1:0] control the integrator time constant according to the following table.

TC[1:0]	time constant
0	.036 ms
1	0.264 ms
2	1.0 ms
3	short caps

A.2. Timing Generator Operation

All signals used by the receiver and provided as outputs are derived from the 5-MHz precision oscillator and a set of counters internal to the AMD9513A timing generator. This device consists of five programmable counters together with load and hold registers and gating circuitry. In addition, a frequency scalar and output divider are provided. All counters and the output divider are operated in binary mode, while the frequency scalar is normally operated in BCD mode. These components are used as described below and in the table.

Name	Pin	Function
SRC1	33	5 MHz frequency standard (5MHZ)
SRC2	32	100-kHz clock (P1)
SRC3-5		not used
GATE1-2		not used
GATE3	36	group interval (GRI)
GATE4	35	envelope gate (PCI)
GATE5	34	special function
OUT1	3	200-kHz clock (P0)
OUT2	2	group interval (GRI)
OUT3	40	code shift (PCX)
OUT4	38	cycle strobe (STB)
OUT5	37	special function
FOUT	7	counter/timer output (J302)

A.2.1. Counter 1 (P0, P1)

Counter 1 counts the 5-MHz precision oscillator to generate a 200-kHz asymmetric square-wave signal (P0) which is further divided by the flipflop IC303A (see Drawing Sheet 4) to generate a 100-kHz signal (P1). Both of these signals are used by the demodulator, which includes internal decoding to generate the four phases required. Counter 1 is operated in Mode J as a variable duty-cycle rate generator with toggled output and no hardware gating. The counter is normally programmed to produce a low interval of 2.4 μs followed by a high interval of 2.6 μs.

A.2.2. Counter 2 (GRI)

Counter 2 counts the 100-kHz output from the external flipflop to generate the group interval signal (GRI) characteristic of the selected LORAN-C chain. The interval is expressed in units of 10 μs, or one cycle time; for instance, 9960 for the Northeast LORAN-C chain. Counter 2 operates in Mode J as a variable duty-cycle rate generator with toggled output and no hardware gating. The counter is normally programmed to generate a low interval equal to the GRI minus 8 ms followed by an a high interval of 8 ms.

A.2.3. Counter 3 (PCX)

Counter 3 counts the 5-MHz precision oscillator to generate the 1-ms phase code clock PCX, from which the envelope gate PCI is derived. It is gated by the GRI signal generated by Counter 2, which persists for 8 ms, or eight 1-ms PCI intervals. The counter is operated in Mode K as a variable duty-cycle rate generator with level gating and toggle output. The counter is normally programmed to generate a low interval of 300 μs followed by a high interval of 700 μs.

A.2.4. Counter 4 (STB)

Counter 4 counts the 5-MHz precision oscillator to generate the 10-μs cycle strobe (STB), which after a programmed delay following the rise of each PCI pulse. This pulse brackets the reference zero-crossing of the pulse group, which is defined as the zero crossing ending the third carrier cycle of each pulse. The counter is operated in Mode L as a hardware-triggered, delayed-pulse, one-shot with edge gating and toggle output. The counter is normally programmed to generate a variable-length low interval followed by a 10-μs high interval..

A.2.5. Counter 5 (OUT)

Counter 5 counts the 5-MHz precision oscillator to drive the frequency scalar and output divider, which produces the output signals for external devices. The counter is operated in Mode K as a variable duty-cycle rate generator with level gating and toggle output. The gating signal is generated by counter 4, which can be enabled for this purpose under program control. When so enabled, counter 5 is stopped for the interval programmed in counter 4, enabling precise alignment of the frequency scalar and output divider to UTC. The counter is normally programmed to generate a low interval of 5 μs followed by a high interval of 5 μs for a frequency of 100 kHz. This output is programmed internally to drive the frequency scalar and output divider, which together divide this frequency by 100,000 to generate the 1-pps output signal. The output signal can also be programmed for almost any submultiple of 5 MHz if UTC alignment is not necessary.

A.3. Interface Connectors

There are five BNC connectors on the receiver and one on the receiver controller. These are intended for use by auxiliary devices, including a monitor oscilloscope. Connectors J201, J203, J204, J205 and J206 are on the receiver, while J301 is on the receiver controller.

A.3.1. J201 (ANT) Antenna/Preamplifier Input

This is the antenna input for either a whip antenna or loop preamplifier. Selection of either type is by switch S201.

A.3.2. J203 (5MHZ) Standard Frequency Output

This is the output of the 5-MHz precision oscillator, which can be connected internally for either sinewave or TTL operation. This output is capable of driving only a high impedance load.

A.3.3. J204 (S1) Q-Integrator Output

This is the demodulated and integrated Q-channel output. This signal ordinarily is connected to the channel-2 vertical deflection circuit of a monitor oscilloscope. This output is capable of driving only a high impedance load.

A.3.4. J205 (PCI) Envelope Gate Output

This is the envelope gate (PCI) signal, which consists of eight 1-ms pulses synchronized to the carrier envelope of the pulse group. This signal ordinarily is connected to the horizontal trigger circuit of a monitor oscilloscope. This output is TTL-compatible.

A.3.5. J206 (SIG) 100-kHz Signal Output

This is the output of the 100-kHz receiver just preceding the synchronous demodulator. This signal ordinarily is connected to the channel-1 vertical deflection circuit of a monitor oscilloscope. This output is capable of driving only a high impedance load.

A.3.6. J301 (OUT) Counter/Timer Output

This is the output of the output divider, which ordinarily consists of a 1-pps pulse synchronized to LORAN-C reference time, but can be programmed for other purposes. This output is TTL-compatible.