ELEG 309 Laboratory 5

MOSFET MEASUREMENT and APPLICATIONS

May 1, 2000

1 Objectives

The overall objective of this Experiment is to familiarize you, the experimenter, with some of the basic properties of MOS transistors, both n and p channel, and to begin the exploration of some of their fundamental applications.

2 Componets and Instrumentation

Our concentration will be on the 4007 MOS array whose package, layout and connections are shown in Fig. 1. As can be seen, the array consists of 6 transistors, 3 p-channel and 3 n-channel, interconnected to some extent in order to reduce the number of IC pins required, but otherwise fairly flexible. One critical point to note is that pins 14 and 7, being the substrate connections of all of the p-channel and all of the n-channel devices, respectively, must be connected appropriately, no matter what use is made of any device. In particular, pin 14 must be connected to the most positive supply in use, and pin 7 to the most negative. Note also that the voltage between pin 14 and pin 7, must be limited to 18 V or so, otherwise internal voltage breakdown may result. For safety's sake, maintain this total supply value at or below 16 V. Other components necessary include resistors of various "unit" values, and a 0.1 μF capacitor, in addition to power-supply filters. A second 4007, if available, can be used to evaluate IC-to-IC device variability as an optional exercise. Instrumentation necessary includes a general-purpose DMM, a dual power supply, a waveform generator and a dual-channel oscilloscope as well as a charactcristic-curve tracer.

3 Reading

The background for this Experiment can be found in Sections 5.1, 5.2, 5.4, 5.5 and 5.6 of the Text.

4 Preparation

Following the usual pattern, Preparation tasks are keyed directly to the Explorations to follow, through the use of the same section numbering and titling.

4.1 Device-integrity checking

4.1.1 Measuring Device Thresholds

For the setup shown in Fig. 2, with the supply voltage adjusted to 10.00 V, the DVM reading (node A to ground) is found to be 8.91 V. Estimate the device-threshold magnitude.

4.1.2 Measuring the Device Conductivity Parameter

For the setup shown in Fig. 2, and the device and situation described above, a 1 kΩ resistor shunting the DVM reduces its reading to 1.53 V. What value of $k_n = \mu_n C_{ox}(W/L)_n$ applies?

4.2 The Amplifier Function

For a transistor for which $V_t = 0.90$ V, $k_n = \mu_n C_{ox}(W/L)_n = 0.6$ mA/V^2, in the circuit of Fig. 4, calculate the values of V_1 and V_2 required to provide $i_D = 0.1$ mA with $v_{DS} = 5$ V.

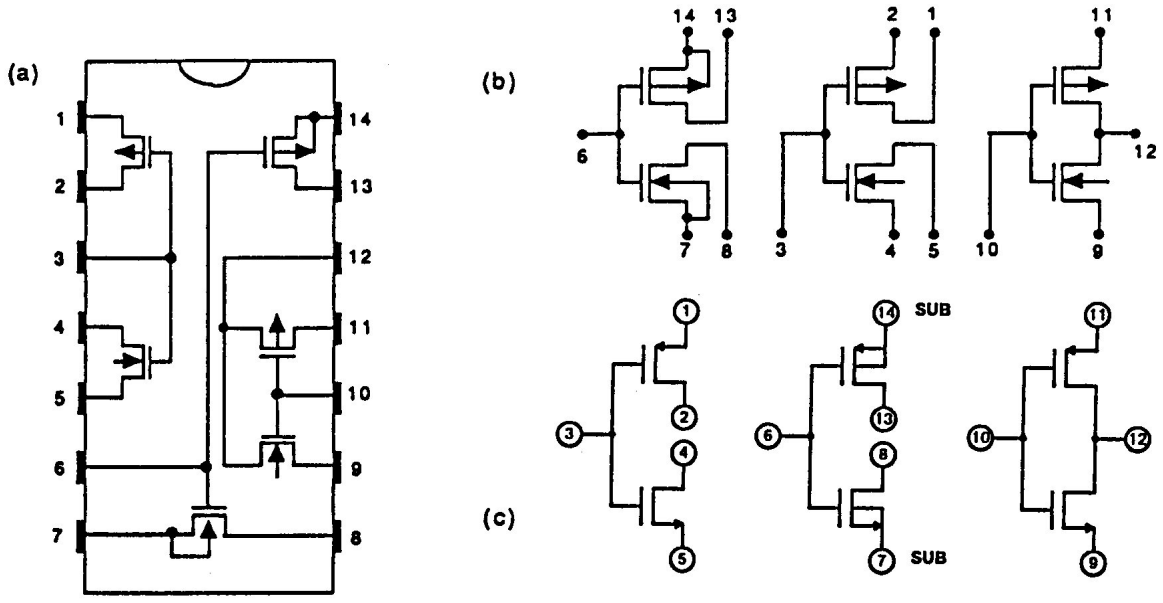

Figure 1: The 4007 MOS Array. a) Base Diagram, top view; b) Pin Assignment; c) Pin Assignment, simplified.

4.2.1 Device Transconductance

For the situation described just above, calculate the value of g_m you can expect. For the 10 kΩ drain resistor, what voltage gain would you get? For a sinewave signal at node I of 1 Vpp, what signal would you expect at node C?

4.3 The Feedback-Bias Topology

4.3.1 A CMOS Active-Loaded Amplifier

- For the circuit of Fig. 5, in which $|V_t| = 1$ V and $k = 0.6$ mA/V^2, find the device drain currents which result, and V_C.
- For $V_A = 30$ V, find g_m, r_o and gain v_d/v_a.
- For what peak output and input signals are the output transistors still in saturation?

4.3.2 Measuring the Input Resistance

- For the situation described above, estimate the input resistance seen to the right of node B. Use the fact (called Miller multiplication) that, for a resistor R connected from output to input of an amplifier of gain A , the corresponding input resistance is $R/(1 - A)$.
- For a signal supplied from node I to node A through a 1 MΩ resistor, what is the gain v_d/v_i which results?

5 Explorations

5.1 Device-Integrity Checking

The purpose of the two Explorations to follow is to introduce techniques for the rapid evaluation of devices in your MOS array. While you may find the ideas involved not directly obvious at first, depending of course on how much and how thoroughly you have read and understood the Text, the basic underlying process is experimentally very simple, and will become clearer as you proceed. What is most important is that you will practice evaluation techniques

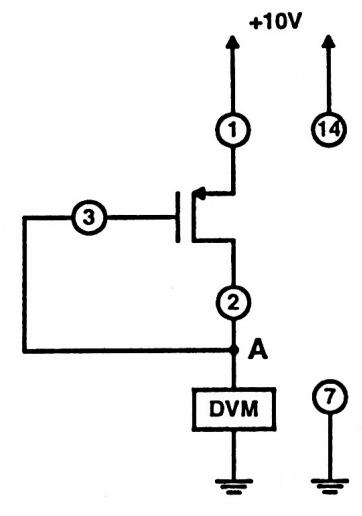

Figure 2: Measurement of V_t for a p-channel device.

which will serve you well later when something does not work as expected, and you wish to verify that your IC still functions.

5.1.1 Measuring Device Thresholds

- **Goal:**To experience, at first hand, how much useful information can be extracted from a simple experiment (in conjunction with sections to follow to follow). Specifically, here, to find V_t quickly.
- **Setup:** Assemble the circuit as shown in Fig. 2 using your array. Ensure that both substrate pins (14 and 7) are connected appropriately. All other pins may be left floating. Ensure that the supply is precisely some convenient value (say 10.00 V), by connecting pins 1 and 2 momentarily (and reading the DVM).
- **Measurement:**
  - Measure the voltage from node A to ground (that is, read the DVM!). Estimate V_t.
  - Repeat the measurement with drain and source interchanged (ie, pin 2 as source and pin 1 as drain).
  - Use your DVM to measure V_{tp} of the other p-channel devices having either pins 6 and 13, or 10 and 12, connected as node A, and with pins 11 and 14 joined (with 1 or 2) to the +10 V supply.
- **Tabulation:** Source-pin #, V_A, V_t.
- **Analysis:** Consider the ease with which you can measure the important device parameter V_t. Note the degree of device-to-device matching and of device symmetry, you have found.

5.1.2 Measuring the Device Conductivity Parameter

- **Goal:** To find k, quickly.
- **Setup:** Use the circuit shown in Fig. 2, the same as above.
- **Measurement:**
  - Short pins 1 and 2 to measure the supply voltage. Set it to some convenient value (eg, 10.00 V).
  - Now, with the short removed, measure the voltage at the drain-gate common connection (node A).

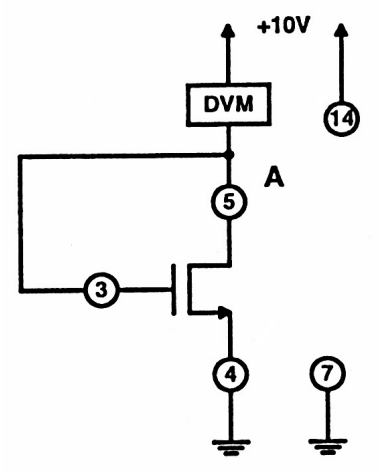

Figure 3: Measurenient of V_t and k for an n-channel device.

  - Now, shunt the DVM with resistors of 10 kΩ or less until the DVM reading lowers by a reasonable amount, say 1 V. Note that a convenient way to do this is to use a (10 kΩ) potentiometer, whose set value is measured subsequently with an ohmmeter. Alternatively, a decade resistor box provides a self-calibrated alternative. Of course, just trying various resistors is OK, since the change does not have to be exact, only measurable. Use the relationship $i_D = 1/2\, k_p(v_{GS} - V_{tp})^2$ from Eq. 5.18 in the Text, to find $k_p = k'_p(W/L)$.

- **Tabulation:** V_{AO}, R, V_{AR}.

- **Analysis:** Consider the ease with which, first V_t then k are found, using a very simple experimental setup. Note that the relatively complex process used here to measure k, leads to a convenient calculation, but is otherwise *not* essential. As noted above, a measurement with any (known) resistor allowing a suitable current flow is all that is needed!

5.1.3 Measuring n-Channel Device Parameters

- **Goal:** To completely characterize an n-channel device, by finding V_t and k_n and to do so in a very simple and direct way.

- **Setup:** Assemble the circuit shown in Fig. 3. Notice the relationship to Fig. 2. Note that the NMOS substrate is grounded through pin 7.

- **Measurement:**

  - First, measure V_{tn} almost directly, as the difference between the supply voltage and the DVM reading.
  - Then, shunting the DVM by some appropriate resistor, say 1 kΩ, find the device voltage, current, and then k_n.

- **Tabulation:** R, V (with computed V_t and k_n), for $R = \infty$ or 1 kΩ.

- **Analysis:** Consider again the ease with which a large amount of information can be found about a MOS device from a very simple experiment.

5.1.4 FET Characteristics

Note: the curve tracer is designed for BJT. In order to use it for FET it is necessary to place a resistor between the gate and the source. If you are not sure what should be the value of the resistor, seek help from your TA.

- **Goal:** To familiarize yourself with the FET family of chararacteristics.

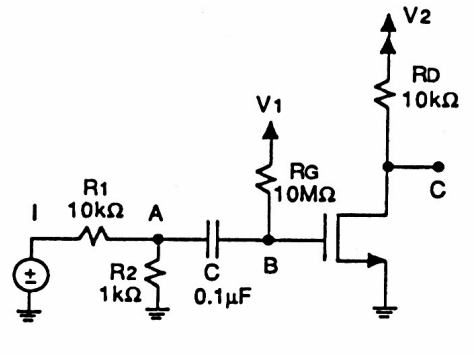

Figure 4: A simple grounded-source amplifier topology.

- **Setup:** Connect one of the FET-s to a curve tracer. Set-up the parameters of the instrument to obtain a reasonable family of curves. Note: make sure the voltage between source and drain does not exceed 16 V.
- **Measurement:** Note the set-up of the curve tracer and the value of the resistor connected between source and drain. Read currents and voltages from the display.
- **Tabulation:** V_G, I_D.
- **Analysis:** Draw in your report the family of characteristics displayed on the curve tracer labeling V_G as necessary. What can you tell about the dependence of the drain current on V_{GS}? Draw the graph of I_D vs. V_G. What is the relationship between them? Read k_n (or k_p) and V_t from the graph.

5.2 The Amplifier Function

We are now going to explore basic amplifier functions, properties and parameters using the circuit of Fig. 4. While this is not an appropriate amplifier topology for most applications, it has the advantages in the present context of simplicity with adaptability. The voltage V_1 is a dc supply whose role it is to adjust the dc component of v_{GS} and hence the dc value of i_D. The voltage V_2 is a second dc supply with which one can control the dc value of v_{DS}, once the value of I_D is established. Capacitor C isolates the dc level at node B, but is large enough (compared to the resistance level at B) to represent a short-circuit for signals in the frequency range of interest.

5.2.1 Device Transconductance

- **Goal:** To evaluate device transconductance.
- **Setup:** Assemble the circuit of Fig. 4 using the 345 NFET (the one whose pins are 3,4,5) with substrates connected to ground and V_2 appropriately.
- **Measurement:**
  - Adjust the signal generator for zero output. With $V_2 = 6$ V, adjust V_1 until $V_C = 5$ V. Measure V_1 (why not V_B?).
  - Apply a 1 Vpp sine wave at 1 kHz to node I, while displaying the voltages at nodes A and C on your oscilloscope. Use ac coupling on the channel connected to node C (for these early measurements). Find the voltage gain $A_v = v_c/v_a$, from node A to node C. Under the assumption that $A_v = g_m R_D$, estimate g_m.
- **Tabulation:** $V_1, I_C, v_b, v_c, v_c/v_b, g_m$.
- **Analysis:** Consider how this value of g_m corresponds to the calculation using Eq. 5.43 in the Text with estimates of V_t and k you have already made.
- **Measurement:**

- With an input signal of zero, raise V_2 to +15 V, and then V_1 until $V_C = 5$ V. Measure V_1 (but not V_B!).
- Now, with a 1 Vpp sine wave at 1 kHz at node I, display and measure the signals on nodes A and C. What is the voltage gain from node A to node C? Estimate g_m.

- **Tabulation:** $V_1, I_C, v_b, v_c, v_c/v_b, g_m$.
- **Analysis:** Consider how the g_m and bias data you have obtained in this Exploration can be used to calculate V_t and k of the transistor you are using. (Hint: Think about Eq. 5.45 and 5.43 of the Text.)

5.2.2 Signal Distortion

- **Goal:** To explore the wave-shape distortion which results with large signals.
- **Setup:** Use the circuit of Fig. 4 with $V_2 = 15$ V and V_1 adjusted so that $V_C = 5$ V, and a 0.1 Vpp triangle wave at 1 kHz applied to node I.
- **Measurement:**
  - Measure nodes A and C, on oscilloscope channel A and B, respectively, with channel B set to ac coupling, and channel A for signal inversion. Adjust the channel A position and gain control channel until the two waveforms exactly overiap.
  - Raise the generator output level, until the input and output waveforms differ by 10% in peak amplitude. Note the peak-to-peak amplitude of the waveform at node C.
  - Switch the node-C channel to dc coupling and measure the dc values of the peaks of the triangle waveform.
- **Analysis:** Consider the nature of the distortion you are seeing: There are two kinds, one a result of the square-law device characteristic (see Eq. 5.32 of the Text), and the other due to operation in the triode region. What kind do you see? How could you demonstrate the other kind? (Hint: Consider changing V_2.)

5.3 The Feedback-bias topology

Our concentration will be on one of the many possible bias techniques that are shown in Fig. 5.39 of the Text, in particular, the one using resistor feedback from drain to gate. There are several reasons for this choice, some practical, some paedogogical: First, this topology allows direct grounding of the source, avoiding the need for a source-bypass capacitor, which must be very large in practice. Second, this topology always guarantees operation of the FET in the saturation region, independent of FET parameters. Third, it extends relatively gracefully from the discrete version to more integrated ones. Fourth, as we shall see, the idea can be generalized to include load biasing as well. Fifth, the resistor from drain to gate directly embodies the idea of feedback, which, as we shall find, is very very important in practical amplifier designs, although often on a more global scale. Finally, though a large resistor is needed, and resistors (particularly large ones) are costly in an IC environment, its value is quite non-critical, making it relatively easier to create with usual IC technologies.

5.3.1 Common Source Active-Load CMOS Amplifier

- **Goal:** To demonstrate the relatively high gain available from an active-loaded CMOS amplifier.
- **Setup:** Assemble the circuit shown in Fig. 5 using Q2, Q3 and Q4 to provide a constant-current load to Q1. Note: the substrate connections are essential!
- **Measurement:**
  - With the supply at 15 V, measure the dc voltages at nodes E and C. Estimate the current in Q1 and its g_m using earlier measured data.
  - With a 0.1 Vpp triangle wave at 10 kHz applied to node A, display the waveforms at nodes C and D. Calculate the gains.
- **Tabulation:** $V_C, v_a, v_c, v_d, v_c/v_a, v_d/v_a$
- **Analysis:** Consider the relatively large gain you find with an active current-source load. How does it compare with a calculation made using g_m and R_L? Consider the effect of r_o of Q1 and Q2? What is the effect of C2 on amplifier performance? [This is easier to see if you lower the input frequency somewhat.]

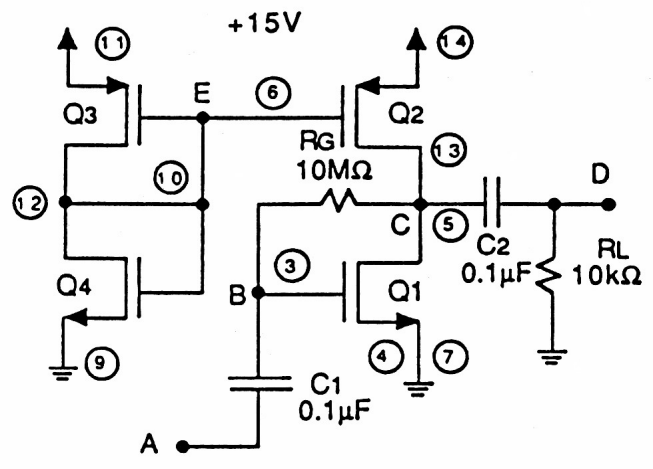

Figure 5: CMOS common-source amplifier.

5.3.2 Nonlinear Distortion

- **Goal:** To evaluate the effects of signal size on amplifier performance.
- **Setup:** Use Fig. 5, as above, with a 0.1 Vpp triangle wave at 10 kHz applied at A.
- **Measurement:**
  - Superimpose the input and output signals (at A, D) by adjusting the gain of the node-A channel appropriately. Note that you may want to use C as the output node to avoid the frequency dependent effects of C2, which tend to "bend" the sides of the triangle wave.)
  - Now, raise the input amplitude, slowly, noting evidence of nonlinearity, then of clipping. At significant events, shift the probe from node D to note the direct-coupled levels at node C.

To be continued...