

ELEG 309 Laboratory 2

OPERATIONAL-AMPLIFIER IMPERFECTIONS and APPLICATIONS

February 25, 2000

1 Objectives

The objective of this Experiment is twofold: First it will familiarize you with important ways in which the integrated-circuit op-amp departs from the ideal. Second, it will allow you to explore, selectively, ways to compensate for some of these deficiencies in applications such as the Miller integrator. You will note that the order of presentation is different from that in the Text in one particular way, a way which is important from an experimental point of view. It is to consider the topics of offsets and offset compensation early, in order that these techniques may be incorporated in later Explorations, where the effects of offsets might otherwise be troublesome.

2 Components and Instrumentation

Your concentration will be on the 741-type op amp provided, one per IC, in an 8-pin dual-in-line (DIP) package whose schematic connection diagram and packaging are shown in Fig. 1. For power, you will use two supplies, +10 V and -10 V, or ± 10 V for short. As well, you need a variety of resistors and capacitors, with emphasis on ones simply specified: $1\text{k}\Omega$, $10\text{k}\Omega$, $100\text{k}\Omega$, $1\text{M}\Omega$, $10\text{M}\Omega$ and $0.1\mu\text{F}$, $0.01\mu\text{F}$, 1nF , and the like. Note that it is important to bypass the two power supplies directly on your prototyping board, using, for each supply, a parallel combination of a $100\mu\text{F}$ tantalum or electrolytic capacitors, and a or $0.1\mu\text{F}$ low-inductance ceramic capacitor. For measurement, you will use a digital multimeter (DMM) with ohms scales, a two-channel oscilloscope, and a waveform generator.

3 Reading

In this Experiment, our concentration will be on Sections 2.4 (particularly 2.4.2), 2.7, 2.8 and 2.9 of the Text. However, as noted above, we will consider the dc problems described in Section 2.9, first, in order that compensation can be considered in later Explorations, as needed. Nevertheless, reading these sections initially in the order presented in the Text, is still a good idea.

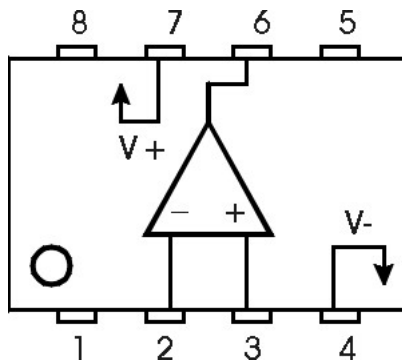


Figure 1: Op-Amp Package and Pin Connections

4 Preparation

This Preparation will be keyed directly to the steps in the Explorations to follow, with direct reference to the circuit figures and procedures found there. Remember to address each of the questions appearing here in your report.

4.1 Voltage and Current Offsets

4.1.1 Offset Measurement

A particular op amp has $V_{OS} = 2$ mV, $I_B = 1.5$ μ A, and I_{OS} is 200 nA, with reference polarities as defined in Fig. 2.35 and Fig. 2.36 of the Text. It is tested in the circuit shown here in Fig. 2, using the resistor values employed in 5.1.1. Find the values of V_C that are observed, namely V_{C1} , V_{C2} , V_{C3} , following the 123 notation of the instruction steps. Note that the polarity of I_{OS} is, in fact, not defined.

4.2 Compensated Miller Integrator

4.2.1 Integrator Offset Control

For the op amp described in above, installed in the circuit of Fig. 3, find the value of V_D that establishes $V_C = 0$ for $V_A = 0$, assuming that the negative input has the higher inward-directed biasing current.

4.2.2 Integrator Operation

- The output of the integrator in Fig. 3, using a 100 nF capacitor, is observed to move linearly from a rest state of -3 V at time 0, to a final state of $+5$ V, 100 μ s later. Describe the input signal that must have been applied.
- For the integrator as above, for what frequency of a sinusoidal input are the input and output of equal size? At what frequency is the output twice the input? What is the phase relation between input and output in each case?

4.3 Frequency Effects

4.3.1 Small-Signal Frequency Response

An inverting amplifier with a nominal closed-loop gain of 100 V/V has a 3dB cutoff at 12.7 kHz. What is its unity gain frequency? What is the 3dB cutoff for a gain of 1000?

4.3.2 Slew-Rate Limiting

- A particular op amp has a 5-V bandwidth of 100 kHz. What is its slew rate?
- For the op amp as above, what is the highest frequency at which a 2 V peak symmetrical triangular wave can be reproduced?

5 Explorations

5.1 Voltage and Current Offsets

5.1.1 Offset Measurement

- **Goal:** To investigate a simple approach to finding bias current, offset current, and offset voltage by indirect measurement using your DVM.
- **Setup:** Assemble the circuit in Figure 2, using ± 10 V supplies, with $R_2 = R_3 = 1$ M Ω .
- **Measurement:** (Use your DVM)
 1. Measure V_C for the circuit as wired.
 2. Short-circuit R_3 , Measure V_C .

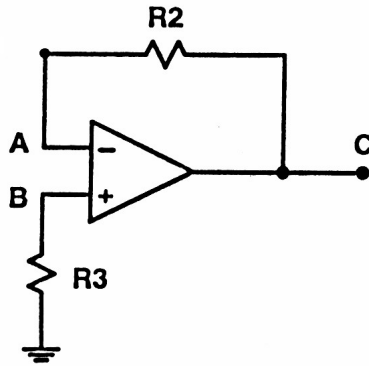


Figure 2: Circuit for the measurement of offsets.

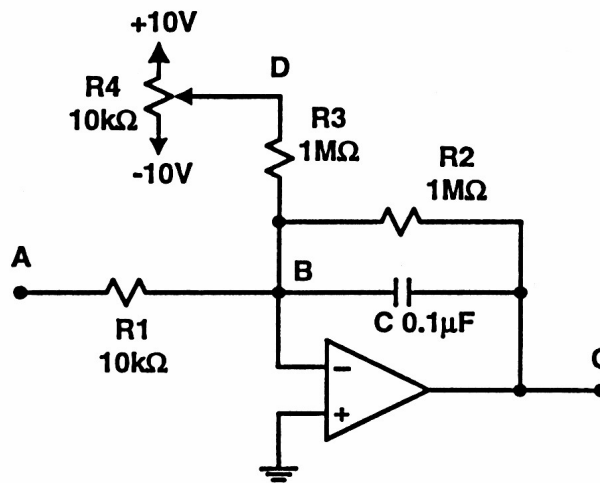


Figure 3: Compensated Integrator.

3. With $R_3 = 0\Omega$, add $R_1 = 1\text{ k}\Omega$ to ground from the negative input. Measure V_C .

- **Tabulation:** V_C, R_1, R_2, R_3 for three situations.
- **Analysis:** Consider the effect of bias current, offset current, and offset voltage on each of these values of V_C , in turn. Estimate each.

5.2 Compensated Miller Integrator

5.2.1 Integrator Offset Control

- **Goal:** To explore a practical way to stabilize an integrator circuit, and then to investigate details of integrator operation.
- **Setup:** Assemble the circuit in Fig. 3 using $\pm 10\text{ V}$ supplies with $R_1 = 10\text{ k}\Omega$, $R_2 = 1\text{ M}\Omega$, $R_3 = 1\text{ M}\Omega$, $R_4 = 10\text{ k}\Omega$, and $C = 0.1\text{ }\mu\text{F}$.
- **Measurement:** (Use your DVM for initial dc measurement, primarily of V_C , and then your oscilloscope for signal measurement)
 1. With node A open, and measuring V_C , adjust R_4 to make $V_C = 0\text{ V}$.

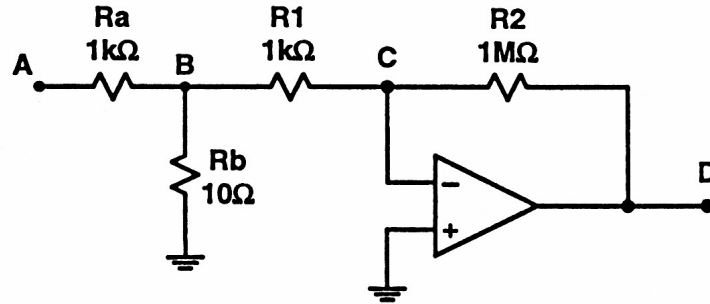


Figure 4: High-Gain Inverting Amplifier for Frequency Measurement.

2. Ground node A. Measure node C and node D.
3. Measure node C. Adjust R_4 to make $V_C = 0$ V. Measure node D.

- **Tabulation:** Node-A status, V_C, V_D
- **Analysis:** Consider what this compensation process can tell you about the offset voltage and bias current of the op amp. Calculate them. What about the offset current?

5.2.2 Integrator Operation

- **Goal:** To illustrate the response of the integrator to square and sinusoidal waveforms.
- **Setup:** Use the circuit as shown in Figure 3 with compensation adjusted as in 5.2.1. Connect a function generator to input A.
- **Measurement:** (Use your dual-channel oscilloscope for these measurements)
 1. Adjust the generator to provide a 1 kHz symmetric square wave at input A of 1 Vpp amplitude. Measure A and C. Sketch the waveforms, noting peak amplitudes and relative timing.
 2. Switch the generator to provide a 1 Vpp sine wave at input A. Sketch the waveforms, noting the peak amplitude and relative timing.
 3. Adjust the generator to find the frequency at which the signals at nodes A and C have the same amplitude. Note the relative phase.
 4. Find the frequencies at which $|v_c/v_a| = 0.1$ and 10.0. Note the relative phase in each case. You may want to adjust the input signal level to make the display more convenient while maintaining a sinewave output.
- **Tabulation:** Waveform shape, peak amplitude, average value, period, time of each zero crossing as measured from an early rising-edge zero crossing of the input. $f_1, \Phi_1, f_2, \Phi_2, f_3, \Phi_3$.
- **Analysis:** Consider the overall operation of the integrator, particularly the amplitude and phase response for sine-wave inputs. Prepare suitable Bode plots.

5.3 Frequency Effects

5.3.1 Small-Signal Frequency Response

- **Goal:** To explore the small-signal frequency effects in an inverting op-amp circuit.
- **Setup:** Assemble the circuit in Figure 4 using ± 10 V supplies. The function generator frequency should be 100 Hz, initially.
- **Measurement:**

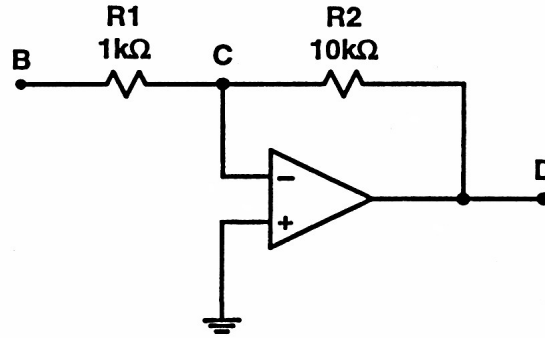


Figure 5: Circuit for Evaluating Slew Rate.

1. Measure nodes A and D. Adjust the generator amplitude to provide a peak output at node D of 1.0 V at 100 Hz.
2. Raise the frequency of the generator to the value at which v_D is reduced by 3 dB (to $1/\sqrt{2} = 0.707$ of its 100 Hz value). Note the frequency as f_4 . Make sure that the voltage at node A has remained at its initial value as established above.
3. Increase the frequency to $10f_4$. Measure the peak output voltage.
4. Change resistor R_2 from 1 M Ω to 100 k Ω and repeat 1, 2, 3.

- **Tabulation:** $R_2, R_2/R_1, f, v_D$ for two values of R_2 and six frequencies.
- **Analysis:** Consider the relationship between closed-loop gain and 3dB bandwidth of the inverting amplifier. [Hint: Read page 95 of the Text.] What is the upper 3dB frequency of each of the amplifiers tested? What is their Gain-Bandwidth Product? Estimate the unity-gain frequency of the op-amp itself. Sketch a Bode amplitude plot showing both of these amplifiers.

5.3.2 Slew-Rate Limiting

- **Goal:** To explore rate-limited behavior of an op-amp output for large signals.
- **Setup:** Assemble the circuit shown in Figure 5.
- **Measurement:**
 1. Measure nodes B and D. For a 1 kHz sinewave input, adjust the input amplitude to provide a 0.1 V peak sinewave at node D.
 2. Raise the frequency to verify that the upper 3dB frequency of this circuit, f_5 , is 100 times that in 5.3.1 (2), namely $100f_4$.
 3. Reduce the frequency to 1 kHz. Raise the input signal until v_D reaches 4 V peak. Note v_B .
 4. Keeping v_B fixed and observing v_D , raise the frequency until v_D falls to 0.707 of its low-frequency value. Note the frequency as f_6 . Sketch the waveform.
 5. Lower v_B to half its former value. What does v_D become?
 6. Raise the frequency to reduce v_D to 0.707 of its value in 5. Note the frequency as f_7 .
- **Tabulation:** v_B, v_D, f for several conditions.
- **Analysis:** Consider the effect of slew-rate on large-signal operation. What is the "4-V bandwidth"? Estimate the full-power bandwidth. Estimate the amplitude of the largest signal that can be used with the expected gain at the small-signal upper 3dB frequency.